1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0014262075	ENGINEERING RELEASED	2018-10-01

J217: MLB-A

LAST_MODIFICATION=Mon Oct 1 11:34:53 2018

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-04062	1	SCHEM,MLB-A,YN,J217	SCH1	CRITICAL	
820-01529	1	PCBF,MLB-A,YN,J217	PCB1	CRITICAL	

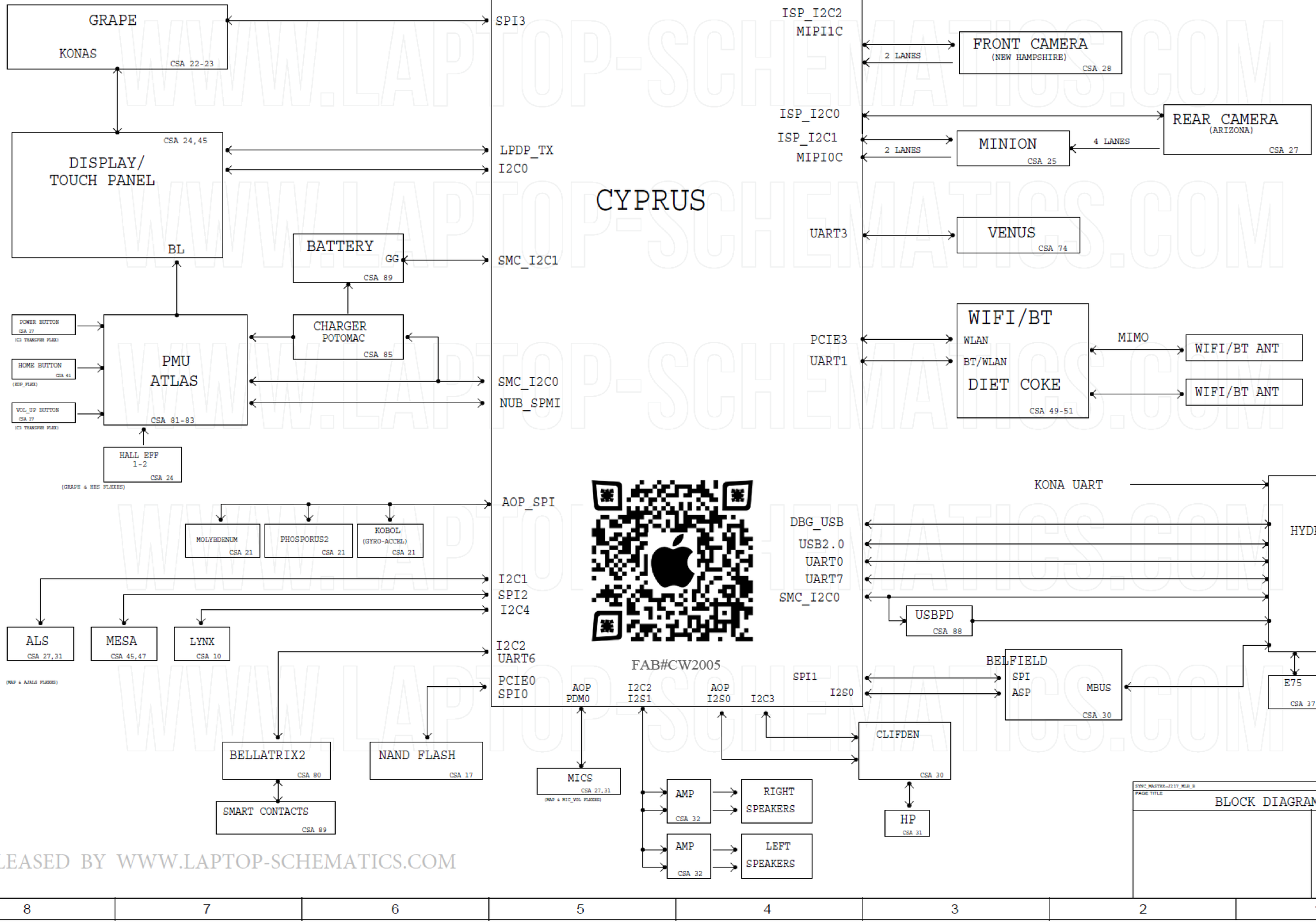
TITLE BLOCK

SYNC_MASTER=J207_MLB_B_ARUBA SYNC_DATE=03/05/2018

DRAWING TITLE

TABLE OF CONTENTS

SCHEM,MLB-A,YN,J217



CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

ALTERNATES

	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
	371S0730	371S00172			D82P0
155S00200		155S00400		FL2860	
	155S00194	155S00400			FL2860
	128S00067	128S00094			C81C0-2
	128S00069	128S00094			C81C0-2
	155S0755	155S00341			FL2700-2,FL4540,FL4710
	131S00172	131S00164			220PF,16V,01005
131S00173		131S00164		C2743,C2801,...	
	376S00159	376S00311			Q8061
	377S0116	377S00132			DZ3540
	138S00116	138S00071			C810D-E,...
	138S00117	138S00071			C810D-E,...
	138S00143	138S00144			C81A0-4,...
	138S00163	138S00144			C81A0-4,...
138S00138		138S00139		C133A-B,...	
	138S00164	138S00139			C133A-B,...
	138S00084	138S00060			C8563-69,...
	152S01037	152S00887			L8101-03,...
	132S00229	132S00010			C8555-57
152S00963		152S00885		L8190,A0	
	372S0194	372S0187			Q3790,Q8990
	376S00319	376S00104			Q2201
	376S00182	376S00126			Q8580
	155S0664	155S00018			FL2742,48,...
152S00964		152S00888		L8121,41	
	152S01003	152S00888			L8121,41

NOMAN'S UPDATED LIST

	131S00299	131S00118			
	132S00232	132S00014			
138S00148		138S00149			
	138S00150	138S00149			
	138S00151	138S00149			
	138S00049	138S0831			
	138S00086	138S0884			
	155S0660	155S0513			
197S00120		197S00118			
	371S0685	371S00176			
	376S1245	376S1102			

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00544	1	POP,CYPRUS+3GB 18NM,B1,M,DEV,CSP1262	U0600	CRITICAL	

PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00545		339S00544	U0600		HYNIX
339S00546		339S00544		U0600	SAMSUNG

NAND

BEST FLASH CONFIGURATIONS (64GB)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00286	1	NAND,3DV3,64GBT,S4E,256G,SD,SLGA110	U1700	CRITICAL	BEST

PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00359		335S00286		U1700	TOSHIBA

ULTIMATE FLASH CONFIGURATIONS (128GB)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00357	1	NAND,3DV3,128GBT,S4E,256G,T,SLGA110	U1700	CRITICAL	ULTIMATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335S00246	335S00357	U1700	WD		

SUPREME FLASH CONFIGURATIONS (256GB)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00247	1	NAND,3DV3,256GBT,S4E,256G,SD,SLGA110	U1700	CRITICAL	SUPREME

PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00358		335S00247	U1700	TOSHIBA	

EXTREME FLASH CONFIGURATIONS (512GB)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00339	1	NAND,3DV4,512GBT,S4E,512G,SD,SLGA110	U1700	CRITICAL	EXTREME

PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00343		335S00339	U1700	HYNIX	

CCG2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S01186	1	PRGM ASSY,IC,CCG2,FW,CYPRESS,V0.3,CSP20	U8809	CRITICAL	

KOBOL

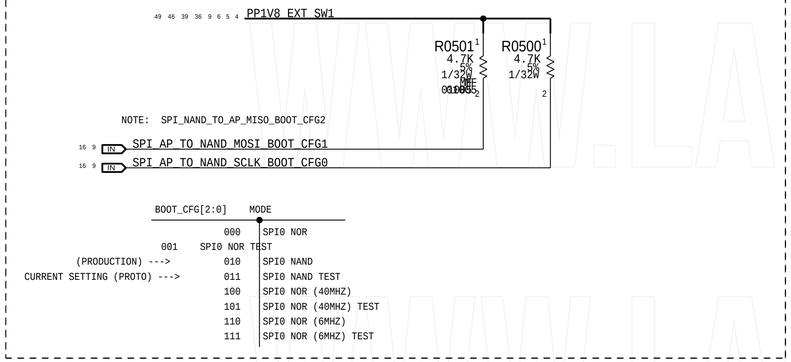
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00367	1	IC,KOBOL,BMI282AA,LGA16	U2150	CRITICAL	KOBOL

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

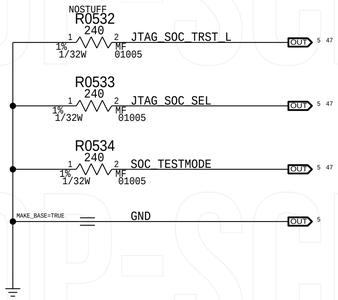
PAGE TITLE

BOM TABLES

BOOT CONFIG ID

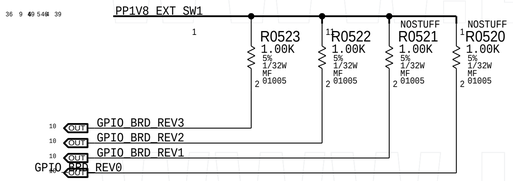


BOOT_CFG[2:0]	MODE
000	SPI0 NOR
001	SPI0 NOR TEST
(PRODUCTION) ---> 010	SPI0 NAND
CURRENT SETTING (PROTO) ---> 011	SPI0 NAND TEST
100	SPI0 NOR (40MHZ)
101	SPI0 NOR (40MHZ) TEST
110	SPI0 NOR (6MHZ)
111	SPI0 NOR (6MHZ) TEST



BOARD REVISION

NOTE: STUFFING RESISTOR MEANS 1



BRD_REV[3-0]	
1111	P1 - NO RCAM SUPPORT
1110	P1 - RCAM SUPPORT
1101	P2 (SKIPPED)
CURRENT SETTING ---> 1100	EVT
1011 TBD	
1010	TBD

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

I2C0

DEVICE	8-BIT	7-BIT
TCON(HIBISCUS)	0X18 - 0X27	
TCON MICRO	0XAC	0X56
TCON TEMP	0X48 - 0X4F	

I2C0_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C0_SCL_1V8 (OUT)
I2C0_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C0_SDA_1V8 (BI)

I2C1

DEVICE	8-BIT	7-BIT
ALS - C4	0X52	0X29
ALS - C3	0X72	0X39

I2C1_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C1_SCL_1V8 (OUT)
I2C1_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C1_SDA_1V8 (BI)

I2C2

DEVICE	8-BIT	7-BIT
SKR AMP CN R	0X72	0X39
SKR AMP CN L	0X74	0X3A
BELLATRIX	0X26	0X13

I2C2_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C2_SCL_1V8 (OUT) ×2
I2C2_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C2_SDA_1V8 (BI) ×2

I2C3

DEVICE	8-BIT	7-BIT
CODEC	0X90	0X48
HYDRA	0X34	0X1A

I2C3_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C3_SCL_1V8 (OUT) ×2
I2C3_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C3_SDA_1V8 (BI) ×2

I2C4

DEVICE	8-BIT	7-BIT
LYNX	0XXX	0XXX

I2C4_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C4_SCL_1V8 (OUT)
I2C4_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C4_SDA_1V8 (BI)

AOP I2C M0

NOT USED

AOP I2C M1

NOT USED

ISP I2C0

DEVICE	8-BIT	7-BIT
RCAM	0X20	0X10

ISP_I2C0_SCL_1V8 (IN) MAKE_BASE=TRUE → ISP_I2C0_SCL_1V8 (OUT)
ISP_I2C0_SDA_1V8 (BI) MAKE_BASE=TRUE → ISP_I2C0_SDA_1V8 (BI)

ISP I2C1

DEVICE	8-BIT	7-BIT
MINION	0X??	0X??

ISP_I2C1_SCL_1V8 (IN) MAKE_BASE=TRUE → ISP_I2C1_SCL_1V8 (OUT)
ISP_I2C1_SDA_1V8 (BI) MAKE_BASE=TRUE → ISP_I2C1_SDA_1V8 (BI)

ISP I2C2

DEVICE	8-BIT	7-BIT
FCAM	0X20	0X10

ISP_I2C2_SCL_1V8 (IN) MAKE_BASE=TRUE → ISP_I2C2_SCL_1V8 (OUT)
ISP_I2C2_SDA_1V8 (BI) MAKE_BASE=TRUE → ISP_I2C2_SDA_1V8 (BI)

ISP I2C3

NOT USED

SMC I2C0

DEVICE	8-BIT	7-BIT
ATLAS	0X78	0X3C
POTOMAC	0XEA	0X75
USBPD	0X24	0X12

I2C_SMC_I2CM0_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C_SMC_I2CM0_SCL_1V8 (OUT) ×3
I2C_SMC_I2CM0_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C_SMC_I2CM0_SDA_1V8 (BI) ×3

SMC I2C1

DEVICE	8-BIT	7-BIT
GASGAUGE	0XAA	0X55

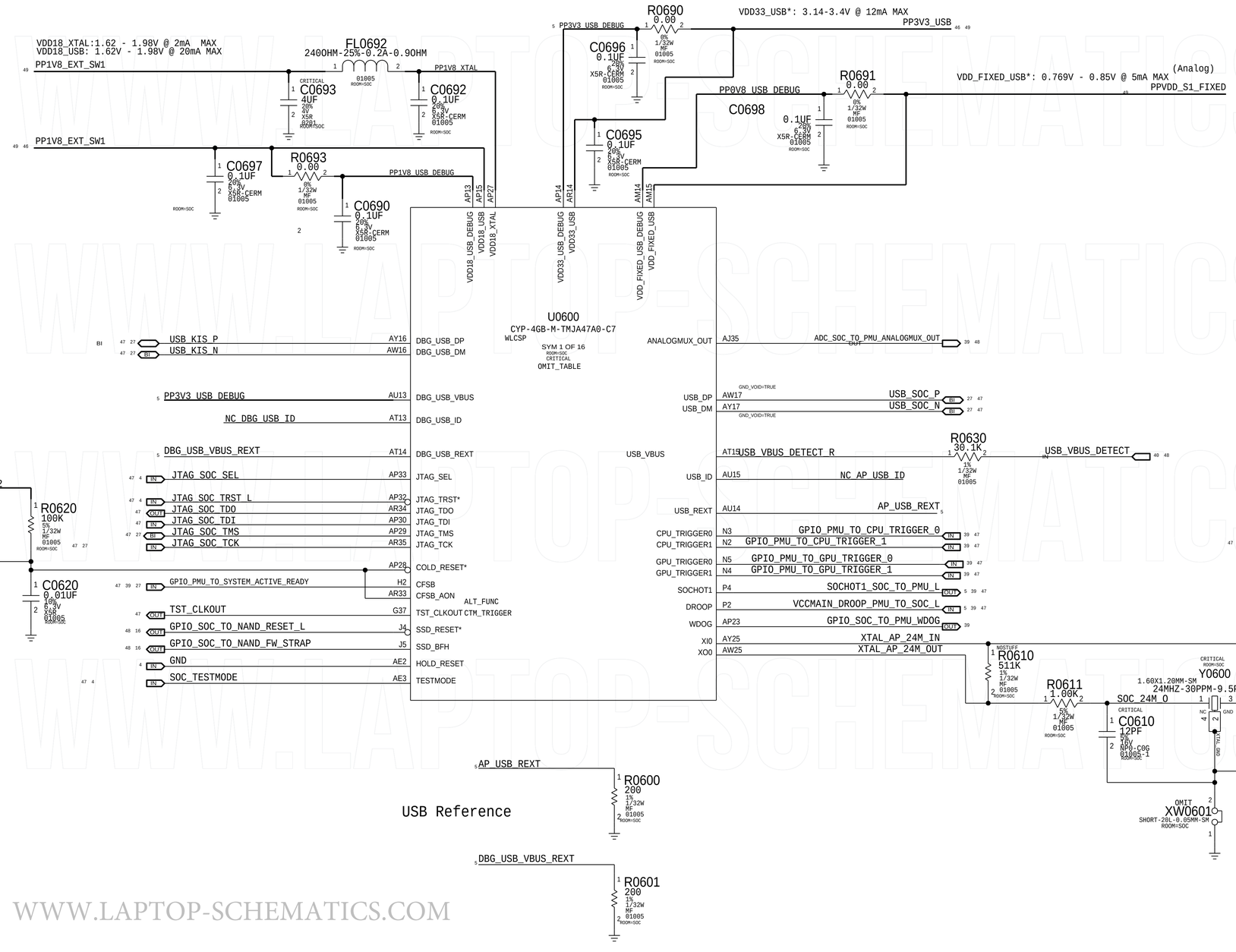
I2C_SMC_I2CM1_SCL_1V8 (IN) MAKE_BASE=TRUE → I2C_SMC_I2CM1_SCL_1V8 (OUT)
I2C_SMC_I2CM1_SDA_1V8 (BI) MAKE_BASE=TRUE → I2C_SMC_I2CM1_SDA_1V8 (BI)

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018

PAGE TITLE

SOC: MISC & ALIASES

SOC - USB, JTAG, XTAL



PAGE TITLE

SOC: JTAG,USB,XTAL

SOC - PCIE

VDD12_PCIE:1.14V - 1.26V @ 60mA MAX
VDD12_PCIE_REFBUF:1.08V - 1.26V @ 20mA MAX

PP1V2_SOC
R0795 0.00 0% 1/32W MF 01005 ROOM=SOC
PP1V2_SOC_PCIE_REFBUF
C0799 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC CRITICAL
C0798 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

VDD_FIXED_PCIE:0.769V - 0.85V @ 60mA MAX
VDD_FIXED_PCIE_REFBUF:0.769V - 0.85V @ 50mA MAX
PPVDD_S1_FIXED
PP0V8_SOC_FIXED_PCIE_REFBUF
R0794 0.00 0% 1/32W MF 01005 ROOM=SOC
C0793 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C0794 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C0791 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC CRITICAL

U0600
CYP-4GB-M-TMJA47A0-C7
WLCSP
SYM 2 OF 16

VDD12_PCIE: AM29, AM31
VDD12_PCIE_REFBUF: AL26, AK27
VDD_FIXED_PCIE0: AL28
VDD_FIXED_PCIE1: AL30
VDD_FIXED_PCIE_REFBUF: AL27

PCIE LINK 0

PCIE_NAND1_TO_SOC_CLKREQ_L	U37	PCIE_CLKREQ0*	PCIE_CLKREQ3*	U34	PCIE_WLAN_TO_SOC_CLKREQ_L
PCIE_SOC_TO_NAND1_REFCLK_P	AW19	PCIE_REF_CLK0_P	PCIE_REF_CLK3_P	AY22	PCIE_SOC_TO_WLAN_REFCLK_P
PCIE_SOC_TO_NAND1_REFCLK_N	AY19	PCIE_REF_CLK0_N	PCIE_REF_CLK3_N	AW22	PCIE_SOC_TO_WLAN_REFCLK_N
PCIE_NAND1_TO_SOC_TX_P	AY27	PCIE_RX0_P	PCIE_RX3_P	AY33	PCIE_WLAN_TO_SOC_TX_P
PCIE_NAND1_TO_SOC_TX_N	AW27	PCIE_RX0_N	PCIE_RX3_N	AW33	PCIE_WLAN_TO_SOC_TX_N
PCIE_SOC_TO_NAND1_TX_C_P	AU26	PCIE_TX0_P	PCIE_TX3_P	AU32	PCIE_SOC_TO_WLAN_TX_C_P
PCIE_SOC_TO_NAND1_TX_C_N	AV26	PCIE_TX0_N	PCIE_TX3_N	AV32	PCIE_SOC_TO_WLAN_TX_C_N
PCIE_SOC_TO_NAND1_RESET_L	T36	PCIE_PERST0*	PCIE_PERST3*	R37	PCIE_SOC_TO_WLAN_RESET_L

C0700 0.22UF 10% CER-X5R 01005 6.3V GND_VOID=TRUE
C0701 0.22UF 10% CER-X5R 01005 6.3V GND_VOID=TRUE
CRITICAL
C0702 0.1UF 20% X5R-CERM 01005 6.3V GND_VOID=TRUE CRITICAL
C0703 0.1UF 20% X5R-CERM 01005 6.3V GND_VOID=TRUE CRITICAL
PCIE_SOC_TO_WLAN_TX_P
PCIE_SOC_TO_WLAN_TX_N

NAND LINK | LINK3

NC_PCIE1_CLKREQ1_L	U36	PCIE_CLKREQ1*	PCIE_CLKREQ2*	U35	NC_PCIE2_CLKREQ2_L
NC_PCIE1_REF_CLK_P	AW20	PCIE_REF_CLK1_P	PCIE_REF_CLK2_P	AY21	NC_PCIE2_REF_CLK_P
NC_PCIE1_REF_CLK_N	AY20	PCIE_REF_CLK1_N	PCIE_REF_CLK2_N	AY21	NC_PCIE2_REF_CLK_N
NC_PCIE1_RX1_P	AY29	PCIE_RX1_P	PCIE_RX2_P	AY31	NC_PCIE2_RX1_P
NC_PCIE1_RX1_N	AW29	PCIE_RX1_N	PCIE_RX2_N	AW31	NC_PCIE2_RX1_N
NC_PCIE1_TX1_P	AU28	PCIE_TX1_P	PCIE_TX2_P	AU30	NC_PCIE2_TX1_P
NC_PCIE1_TX1_N	AV28	PCIE_TX1_N	PCIE_TX2_N	AV30	NC_PCIE2_TX1_N
NC_PCIE1_PERST1_L	T35	PCIE_PERST1*	PCIE_PERST2*	T34	NC_PCIE2_PERST2_L

LINK1 | LINK2

PCIE_RCAL_POS AR31 — R0740 200 1% 1/32W MF 01005 ROOM=SOC — PCIE_RCAL_NEG
C0740 10PF 5% 16V CERM 01005 ROOM=SOC CRITICAL

PCIE_RCAL_POS	AT31	PCIE_RCAL_P		
PCIE_RCAL_NEG		PCIE_RCAL_N		
			PCIE_CLKREQ4*	T37	NC_PCIE_AP_BI_BB_CLKREQ_L
			PCIE_REF_CLK4_P	AY23	NC_90_PCIE_AP_TO_BB_REFCLK_P
			PCIE_REF_CLK4_N	AW23	NC_90_PCIE_AP_TO_BB_REFCLK_N
			PCIE_RX4_P	AY35	NC_90_PCIE_BB_TO_AP_TX_P
			PCIE_RX4_N	AW35	NC_90_PCIE_BB_TO_AP_TX_N
			PCIE_TX4_P	AU34	NC_90_PCIE_AP_TO_BB_TX_P
			PCIE_TX4_N	AV34	NC_90_PCIE_AP_TO_BB_TX_N
			PCIE_PERST4*	R35	NC_PCIE_AP_TO_BB_PERST_L

LINK4

PCIE LINK 3
PCIE LINK 4

PCIe BB CLKREQ PU on BB domain
PCIe Clock Request Pull-Ups

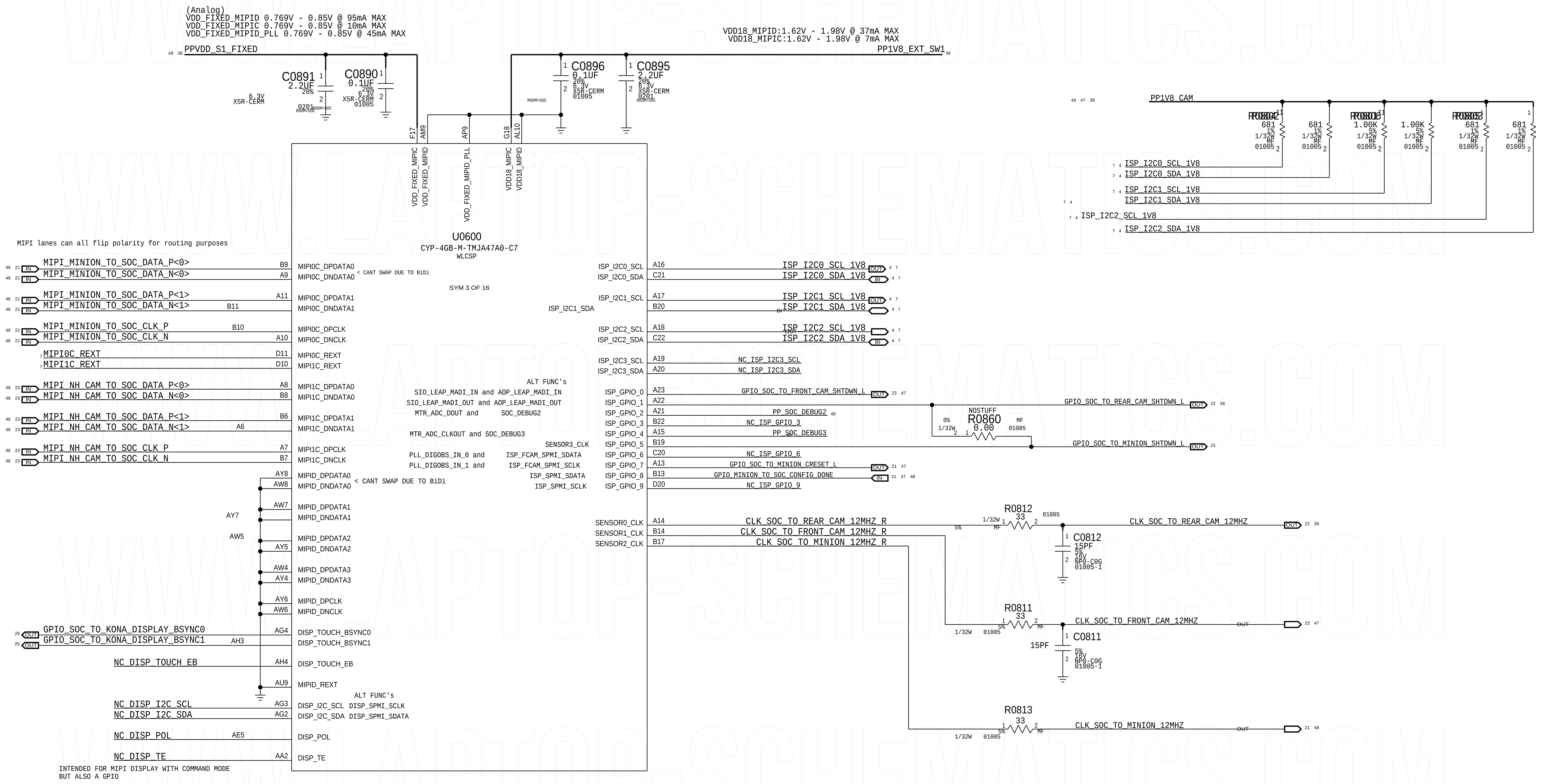
PP1V8_EXT_SW1
R0700 100K 5% 1/32W MF 01005 ROOM=SOC
R0730 100K 5% 1/32W MF 01005 ROOM=SOC
PCIE_NAND1_TO_SOC_CLKREQ_L
PCIE_WLAN_TO_SOC_CLKREQ_L

PCIe Reset Pull-Downs

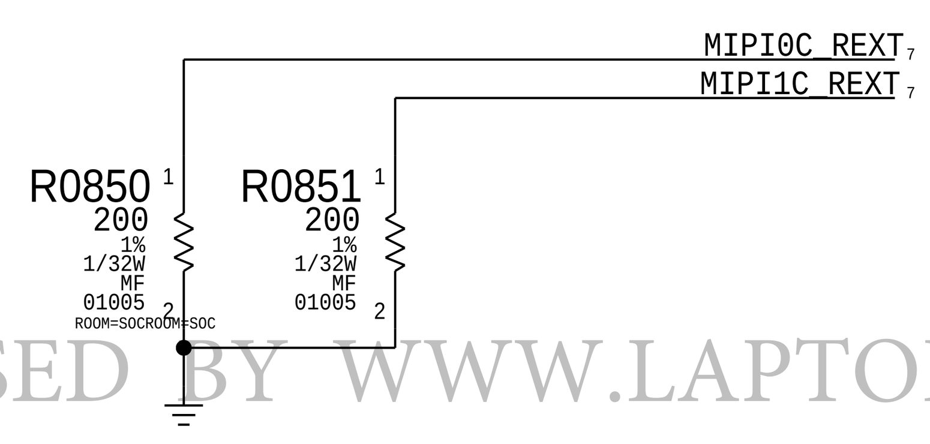
PCIE_SOC_TO_WLAN_RESET_L
PCIE_SOC_TO_NAND1_RESET_L
R0701 100K 5% 1/32W MF 01005 ROOM=SOC
R0731 100K 5% 1/32W MF 01005 ROOM=SOC

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
SOC: PCIE

SOC - MIPI



MIPI Reference



SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

SOC: MIPI

SOC - LPDP

VDD12_PLL_LPDP 1.14V - 1.26V @ 9mA MAX
VDD12_LPDP_RX 1.14V - 1.26V @ 115mA MAX
PP1V2_SOC
49

C0990 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C0991 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C0992 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C0993 0.01UF 10% 6.3V X5R 01005 ROOM=SOC
C0994 15PF 5% 16V NP0-C0G 01005-1 ROOM=SOC
Desense for Wifi frequencies

GND'd offpage
GND'd offpage

(Analog)
VDD_FIXED_PLL_LPDP 0.769V - 0.85V @ 3mA MAX
VDD_FIXED_LPDP_RX 0.769V - 0.85V @ 30mA MAX
PPVDD_S1_FIXED
36 49

C0995 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C0996 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

F27 VDD12_LPDP_TX
F29 VDD12_LPDP_RX
AM10 VDD12_PLL_LPDP
AM13 VDD_FIXED_PLL_LPDP
R11 VDD_FIXED_LPDP_TX
G28 VDD_FIXED_LPDP_RX

U0600
CYP-4GB-M-TMJA47A0-C7
WLCSP
SYM 4 OF 16

A25	LPDPRX_RX_D0_P		LPDP_TX0P	AY14	LPDP_SOC_TO_TCON_DATA_P<0>	OUT 30
B25	LPDPRX_RX_D0_N		LPDP_TX0N	AW14	LPDP_SOC_TO_TCON_DATA_N<0>	OUT 30
B26	LPDPRX_RX_D1_P		LPDP_TX1P	AY13	LPDP_SOC_TO_TCON_DATA_P<1>	OUT 30
C26	LPDPRX_RX_D1_N		LPDP_TX1N	AW13	LPDP_SOC_TO_TCON_DATA_N<1>	OUT 30
A27	LPDPRX_RX_D2_P		LPDP_TX2P	AY12	LPDP_SOC_TO_TCON_DATA_P<2>	OUT 30
B27	LPDPRX_RX_D2_N		LPDP_TX2N	AW12	LPDP_SOC_TO_TCON_DATA_N<2>	OUT 30
B28	LPDPRX_RX_D3_P		LPDP_TX3P	AY11	LPDP_SOC_TO_TCON_DATA_P<3>	OUT 30
C28	LPDPRX_RX_D3_N		LPDP_TX3N	AW11	LPDP_SOC_TO_TCON_DATA_N<3>	OUT 30
B30	LPDPRX_RX_D4_P					
C30	LPDPRX_RX_D4_N					
A31	LPDPRX_RX_D5_P		LPDP_AUX_P	AY10	LPDP_SOC_TO_TCON_AUX_P	BI 30
B31	LPDPRX_RX_D5_N		LPDP_AUX_N	AW10	LPDP_SOC_TO_TCON_AUX_N	BI 30
B32	LPDPRX_RX_D6_P					
C32	LPDPRX_RX_D6_N		EDP_HPD	AF2	LPDP_TCON_TO_SOC_HPD	IN 30 47
			DP_WAKEUP	AF4	NC_DP_WAKEUP	
A33	LPDPRX_RX_D7_P					
B33	LPDPRX_RX_D7_N					

NC_LPDP_D0_AUX	D23	LPDPRX_AUX_D0_P	
NC_LPDP_D1_AUX	D24	LPDPRX_AUX_D1_P	
NC_LPDP_D2_AUX	C24	LPDPRX_AUX_D2_P	
NC_LPDP_D3_AUX	D25	LPDPRX_AUX_D3_P	
NC_LPDP_D4_AUX	D27	LPDPRX_AUX_D4_P	
NC_LPDP_D5_AUX	D29	LPDPRX_AUX_D5_P	
NC_LPDP_D6_AUX	D31	LPDPRX_AUX_D6_P	
NC_LPDP_D7_AUX	D33	LPDPRX_AUX_D7_P	

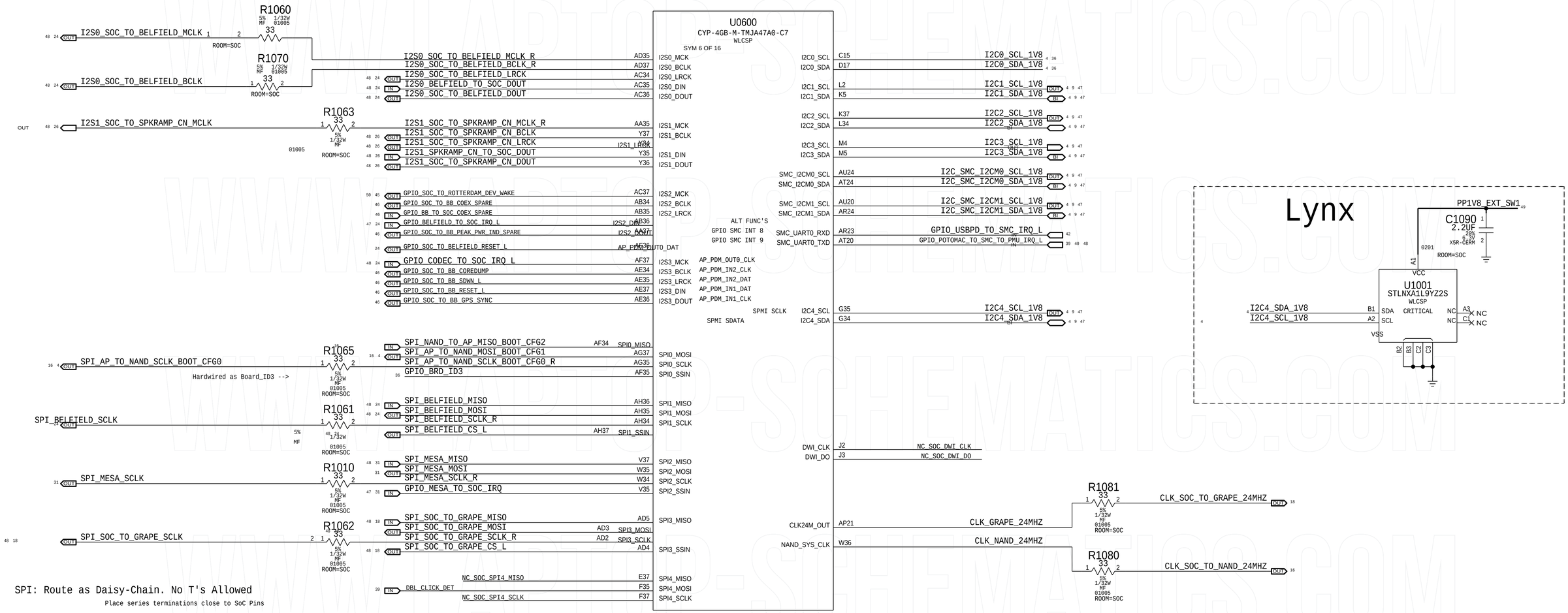
OK PER SANJEEV MAHESHWARI (3/9/18)

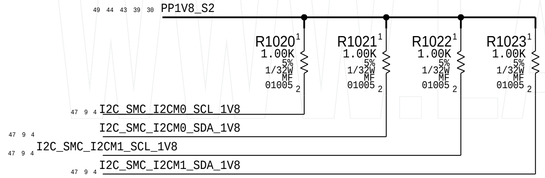
NC_LPDPRX_RCAL_POS	A29	LPDPRX_RCAL_P	LPDP_RCAL_P	AU10	LPDP_RCAL_POS
NC_LPDPRX_RCAL_NEG	B29	LPDPRX_RCAL_N	LPDP_RCAL_N	AT10	LPDP_RCAL_NEG

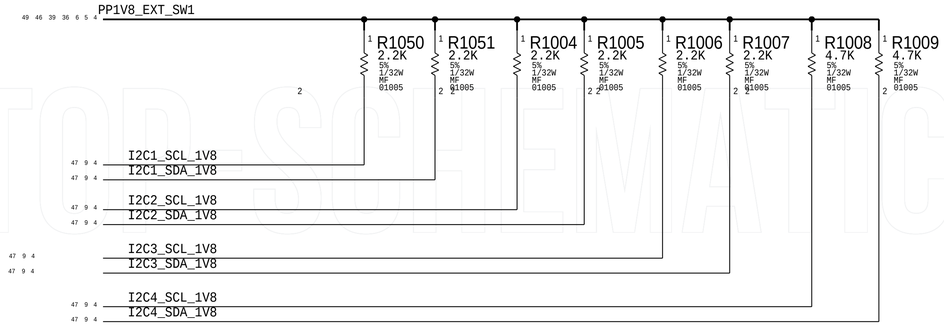
R0901 200 1% 1/32W MF 01005 ROOM=SOC
C0902 10PF 5% CERM 16V 01005 ROOM=SOC

PAGE TITLE
SOC: LPDP

SOC - SERIAL INTERFACES



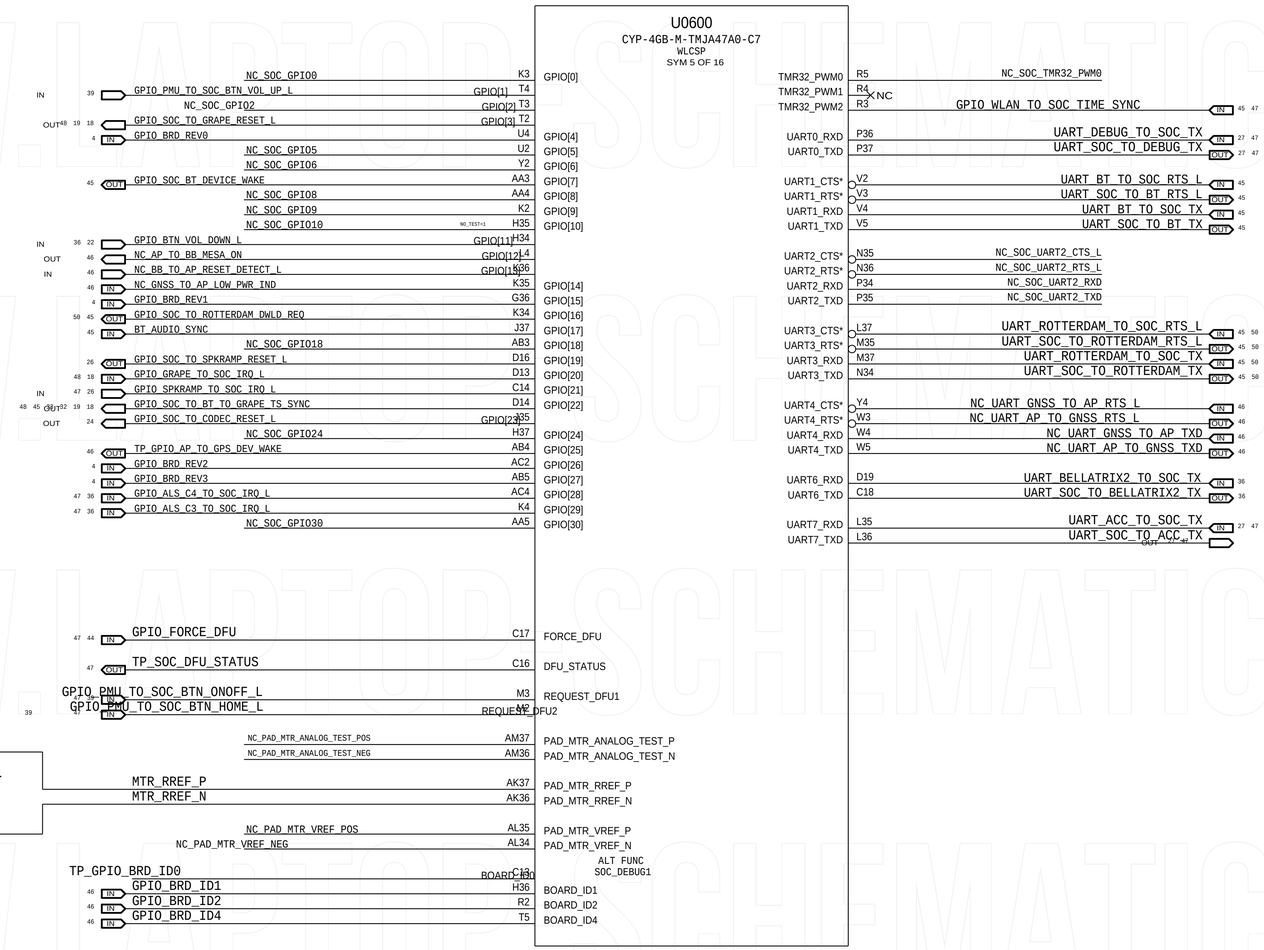




PAGE TITLE

SOC: SERIAL

SOC - GPIO INTERFACES



PAGE TITLE

SOC: GPIO & UART

SOC - AOP

1.62V - 1.98V @ 10mA MAX
PP1V8_S2
C1290 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1291 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
VDDIO18_AOP
U0600 CYP-4GB-M-TMJA47A0-C7 WLCSP SYM 7 OF 16

ALT FUNC's
AOP_LPPLL
AOP_PDM_CLK4
AOP_PDM_CLK3
ALT FUNC
AOP_PDM_CLK2

PP_SOC_AON_SLEEP1_RESET_L	AU21	AON_SLEEP1_RESET*	
NC_AOP_FUNC0	AP8	AOP_FUNC[0]	<-- SCM_SPI CS & Trig
NC_AOP_FUNC1	AP10	AOP_FUNC[1]	
NC_AOP_FUNC2	AT6	AOP_FUNC[2]	
NC_AOP_FUNC3	AR8	AOP_FUNC[3]	
SPI_KOBOL_CS_L	AT17	AOP_FUNC[4]	
GPIO_PHOSPHORUS_TO_AOP_IRQ	AU17	AOP_FUNC[5]	
SPI_PHOSPHORUS_CS_L	AP18	AOP_FUNC[6]	
NC_AOP_FUNC7	AR9	AOP_FUNC[7]	
NC_AOP_FUNC8	AP12	AOP_FUNC[8]	
GPIO_ORION_TO_AOP_IRQ	AR11	AOP_FUNC[9]	
GPIO_AOP_TO_ORION_HWEN	AU17	AOP_FUNC[10]	
SPI_MOLY_CS_L	AR15	AOP_FUNC[11]	
GPIO_KOBOL_TO_AOP_INT	AR12	AOP_FUNC[12]	<SCM_I2CM0_TRIGGER
NC_AOP_FUNC13	AT7	AOP_FUNC[13] AOP_I2CM1_SCL	
GPIO_MOLY_TO_AOP_IRQ	AR18	AOP_FUNC[14] AOP_I2CM1_SDA	
GPIO_KOBOL_TO_AOP_MOTION_INT	AT8	AOP_FUNC[15]	
NC_AOP_FUNC16	AP19	AOP_FUNC[16]	
NC_AOP_FUNC17	AT18	AOP_FUNC[17]	
NC_AOP_FUNC18	AT8	AOP_FUNC[18]	
NC_AOP_FUNC19	AU18	AOP_FUNC[19]	<SCM_I2CM1 TRIGGER
NC_AOP_FUNC20	AT11	AOP_FUNC[20]	
GPIO_AOP_TO_WLAN_CONTEXT_B	AU4	AOP_FUNC[21]	
NC_AOP_FUNC22	AT12	AOP_FUNC[22]	
SPI_SENSORS_MISO	AP6	AOP_SPI_MISO	
SPI_SENSORS_MOSI_R	AP7	AOP_SPI_MOSI	
SPI_SENSORS_SCLK_R	AP16	AOP_SPI_SCLK	
NC_UART_BB_TO_AOP_TXD	AR5	AOP_UART0_RXD	
NC_UART_AOP_TO_BB_TXD	AR6	AOP_UART0_TXD	
NC_AOP_UART1_RXD	AU16	AOP_UART1_RXD	
NC_AOP_UART1_TXD	AT19	AOP_UART1_TXD	
GPIO_PMU_TO_SOC_IRQ_L	AR4	AOP_UART2_RXD	
GPIO_AOP_TO_WLAN_CONTEXT_A	AT4	AOP_UART2_TXD	
I2S_AOP_TO_CODEC_BCLK_R	AU11	AOP_I2S0_BCLK	
I2S_CODEC_TO_AOP_DOUT	AU19	AOP_I2S0_DIN	
NC_AOP_I2S0_MCK	AR20	AOP_I2S0_MCK	AOP_PDM_CLK2
I2S_AOP_TO_CODEC_LRCK	AU7	AOP_I2S0_LRCK	
I2S_AOP_TO_CODEC_DOUT	AU8	AOP_I2S0_DOUT	ALT FUNC's
NC_AOP_I2S1_BCLK	AU5	AOP_I2S1_BCLK	AOP_PDM_IN1_CLK
NC_AOP_I2S1_DIN	AT10	AOP_I2S1_DIN	
NC_AOP_I2S1_MCK	AU12	AOP_I2S1_MCK	
NC_AOP_I2S1_LRCK	AU6	AOP_I2S1_LRCK	AOP_PDM_IN2_CLK
NC_AOP_I2S1_DOUT	AP20	AOP_I2S1_DOUT	AOP_PDM_IN2_DAT

AOP_PDM_CLK0	AT21		DMIC1_MIC_SCLK (OUT)
AOP_PDM_DATA0	AT22		DMIC1_MIC_SD (IN)
AOP_PDM_DATA1	AU23	NC_AOP_PDM_DATA1	
RT_CLK32768	AP26		CLK_PMU_TO_AOP_32K (IN)
SWD_TMS2	C19		SWD_NAND1_SWDIO (BI)
SWD_TMS3	B16		SWD_GRAPE_SWDIO (BI)
AOP_I2CM0_SCL	AP17	NC_AOP_I2CM0_SCL	
AOP_I2CM0_SDA	AP5	NC_AOP_I2CM0_SDA	
AOP_I2CM1_SCL	AR17	NC_AOP_I2CM1_SCL	
AOP_I2CM1_SDA	AT5	NC_AOP_I2CM1_SDA	
AOP_PDM_OUT0_CLK	AT23	NC_AOP_PDM_OUT0_CLK	
AOP_PDM_DATAOUT	AU22	NC_AOP_PDM_DATAOUT	
NUB_DOCK_CONNECT	AR27		USB_TO_SOC_DOCK_CONNECT (IN)
NUB_DOCK_ATTENTION	AP25		GPIO_HYDRA_TO_SMC_IRQ (IN)
NUB_SWD_TCK_OUT	AP24		SWD_PERIPHERAL_SWCLK
NUB_SPMI_SCLK	AR21		NUB_SPMI_ATLAS_SCLK
NUB_SPMI_SDATA	AR29		NUB_SPMI_ATLAS_SDATA
NUB_SWD_TMS0	AR26		NC_SWD_JTAG_BB_TMS_SWDIO (BI)
NUB_SWD_TMS1	AP22		SWD_USBPD_SWDIO (BI)

ALT FUNC's
NUB_PDM_CLK1

PP1V8_GRAPE
PP1V8_EXT_SW1
R1216 1.00K 5% 1/32W MF 01005
R1217 1.00K 5% 1/32W MF 01005
SWD_NAND1_SWDIO
SWD_GRAPE_SWDIO

PP1V8_S2
NOSTUFF R1240 1.00K 5% 1/32W MF 01005
SWD_USBPD_SWDIO

R1230 33 5% 1/32W MF 01005 ROOM=SOC — SPI_SENSORS_MOSI
R1201 33 5% 1/32W MF 01005 ROOM=SOC — SPI_SENSORS_SCLK
R1231 33 5% 1/32W MF 01005 ROOM=SOC — I2S_AOP_TO_CODEC_BCLK

THESE GATES HAVE BACKPOWER PROTECTION

PP1V8_S2
C1250 0.1UF 20% 6.3V X5R-CERM 01005
U1250 74AUP1G34GX SOT1226
R1250 33 5% 1/32W MF 01005 — SWD_PERIPHERAL_SWCLK — SWD_PER_USBPD_SWCLK_R
R1251 33 5% 1/32W MF 01005 — SWD_USBPD_SWCLK_R — SWD_USBPD_SWCLK

THESE GATES HAVE BACKPOWER PROTECTION

PP1V8_EXT_SW1
C1220 0.1UF 20% 6.3V X5R-CERM 01005
U1200 74AUP1G34GX SOT1226
R1220 33 5% 1/32W MF 01005 — SWD_PERIPHERAL_SWCLK — SWD_PER_NAND1_SWCLK_R — SWD_NAND1_SWCLK

PP1V8_GRAPE
C1221 0.1UF 20% 6.3V X5R-CERM 01005
U1201 74AUP1G34GX SOT1226
R1221 33 5% 1/32W MF 01005 — SWD_PERIPHERAL_SWCLK — SWD_PER_GRAPE_SWCLK_R — SWD_GRAPE_SWCLK

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
SOC: AOP

SOC - CPU, GPU & SOC RAILS

Remote sense XW's for Buck0 Buck1 and Buck11 live off page for dev board compapability

1.06V @ 13.8A MAX
0.905V @ 8.9A MAX
0.527V @ 1.6A MAX
PPVDD_CPU

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WLCSP
SYM 8 OF 16

VDD_PCPU
VDD_LOW
VDD_LOW_ULPPLL
VDD_LOW_FLPPLL
VDD_CPU_SRAM
VDD_GPU_SRAM

VDD_LOW: 0.691V - 0.756V @ 220mA MAX
VDD_LOW_ULPPLL: 0.691V - 0.756V @ 0.3mA MAX
VDD_LOW_FLPPLL: 0.691V - 0.756V @ 0.03mA MAX
PP0V75_S2_A0P

PP0V7_VDD_LOW_ULPPLL_R
PP0V7_VDD_LOW_FLPPLL_R

1.02V @ 2.1A MAX
0.975V @ 1.4A MAX
0.765V @ 0.33A MAX
PPVDD_CPU_SRAM

1.06V @ 1.6A MAX
0.725V @ 1.1A MAX
0.685V @ 1.03A MAX
PPVDD_GPU_SRAM

1.06V @ 10.5A MAX
0.725V @ 6.3A MAX
0.570V @ 3.1A MAX
PPVDD_GPU

VDD_GPU

1.00V @ 2.9A MAX
0.750V @ 1.9A MAX
0.07V @ 1.14A MAX
PPVDD_ECPU

VDD_ECPU

VDD_FIXED_PCPU: 0.769 - 0.85V @ 5mA
VDD_FIXED_MTR 0.769V - 0.85V @ 1mA
VDD_FIXED_ECPU: 0.769V - 0.85V @ 5mA
VDD_FIXED_PLL_SOC: 0.81V @ 9mA
VDD_FIXED_PLL_ANE: 0.81V @ 5mA
VDD_FIXED_PLL_GPU: 0.81V @ 5mA
VDD_FIXED_PLL_DDR*: 0.81V @ 8mA

VDD12_PLL_SOC: 1.14 - 1.26V @ 8mA MAX
VDD12_PLL_ANE: 1.14 - 1.26V @ 4mA MAX
VDD12_PLL_PCPU: 1.14 - 1.26V @ 4mA MAX
VDD12_PLL_ECPU: 1.14 - 1.26V @ 4mA MAX
VDD12_PLL_GPU: 1.14 - 1.26V @ 4mA MAX
PP1V2_SOC

0.783V @ 4.2A MAX
0.661V @ 2.6A MAX
0.595V @ 2.1A MAX
PPVDD_S1_SOC

VDD_SOC

PPVDD_S1_FIXED

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/03/2018
PAGE TITLE
SOC: POWER (1/3)

SOC - CPU, GPU & SOC RAILS

0.81V @ 900mA MAX
PPVDD_S1_FIXED

C1401 14UF 20% 4V X5R 0402-D2X-1

C1402 4UF 20% 4V X5R 0201 ROOM=SOC
C1403 4UF 20% 4V X5R 0201 ROOM=SOC
C1404 4UF 20% 4V X5R 0201 ROOM=SOC
C1405 4UF 20% 4V X5R 0201 ROOM=SOC

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VDD_FIXED
VDD_FIXED

ADC_SOC_TO_PMU_VDD_GPU → P21 VDD_GPU_SENSE
ADC_SOC_TO_PMU_VDD_CPU → AG16 VDD_PCPU_SENSE
ADC_SOC_TO_PMU_VDD_SOC → AH21 VDD_SOC_SENSE

VSS_GPU_SENSE P22 → GPU_SENSE_NEG
VSS_PCPU_SENSE AH16 → CPU_PCORE_SENSE_NEG
VSS_SENSE AH20 → SOC_SENSE_NEG
VSS_DDR_SENSE B4 → VDDQL_DCS_SENSE_NEG

VDDQL* TOTAL: 0.60V - 0.63V @ 620mA MAX
PPVDD_S1_QL

C1490 4UF 20% 4V X5R 0201 ROOM=SOC
C1430 4UF 20% 4V X5R 0201 ROOM=SOC
C1431 4UF 20% 4V X5R 0201 ROOM=SOC
C1432 4UF 20% 4V X5R 0201 ROOM=SOC
C1433 4UF 20% 4V X5R 0201 ROOM=SOC

Place caps on SoC Corners

C1492 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

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VDDQL_DDR0
VDDQL_DDR1
VDDQL_DDR2
VDDQL_DDR3

VDDQL_SENSE_POS → C4 VDDQL_SENSE
PP1V1_S2 → VDDIO11_RET_DDR0 / VDDIO11_RET_DDR1 / VDDIO11_RET_DDR2 / VDDIO11_RET_DDR3
Current included in VDD2

RESET_PMU_TO_SYSTEM_L → AL3 LP4_IN_RESET*
rdar#: 29795211, This pin replaces the 4 DDR* sys alive pins

VDD_DCS_DDR0
VDD_DCS_DDR1
VDD_DCS_DDR2
VDD_DCS_DDR3
VDD_DCS_SENSE

1.00V @ 1.14A MAX
0.85V @ 750mA MAX
0.70V @ 430mA MAX
PPVDD_S1_DCS

C1460 4UF 20% 4V X5R 0201 ROOM=SOC
C1461 4UF 20% 4V X5R 0201 ROOM=SOC
C1462 4UF 20% 4V X5R 0201 ROOM=SOC
C1463 4UF 20% 4V X5R 0201 ROOM=SOC

Place caps on SoC Corners

DCS_SENSE_POS

DDR IMPEDANCE CONTROL
PPVDD_S1_QL

R1460 240 1% 1/32W MF 0100S ROOM=SOC
R1461 240 1% 1/32W MF 0100S ROOM=SOC
R1462 240 1% 1/32W MF 0100S ROOM=SOC
R1463 240 1% 1/32W MF 0100S ROOM=SOC
R1470 240 1% 1/32W MF 0100S ROOM=SOC
R1471 240 1% 1/32W MF 0100S ROOM=SOC

DDR0_RREF AL4 DDR0_RREF
DDR1_RREF AN35 DDR1_RREF
DDR2_RREF G4 DDR2_RREF
DDR3_RREF D35 DDR3_RREF

DDR0_ZQ AH2 DDR0_ZQ
DDR3_ZQ DDR3_ZQ

VDD1_DDR* : 1.70V - 1.95V @ 220mA MAX
PP1V8_S2

VDD1_DDR0 AA1 AV2
VDD1_DDR1 AA38 AV37
VDD1_DDR2 C2 Y1
VDD1_DDR3 C37 Y38

C1450 4UF 20% 4V X5R 0201 ROOM=SOC
C1451 4UF 20% 4V X5R 0201 ROOM=SOC
C1452 4UF 20% 4V X5R 0201 ROOM=SOC
C1453 4UF 20% 4V X5R 0201 ROOM=SOC

VDD2_DDR* : 1.06V - 1.17V @ 2.2A MAX
PP1V1_S2

VDD2_DDR0 AB2 AH1 AK1 AM1 AU3
VDD2_DDR1 AB37 AH38 AK38 AM38 AU36
VDD2_DDR2 D3 J1 L1 N1 W2
VDD2_DDR3 D36 J38 L38 N38 W37

C1440 6.3V
C1441 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1442 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1443 2.2UF 20% X5R-CERM 0201 ROOM=SOC
C1480 2.2UF 20% X5R-CERM 0201 ROOM=SOC
4UF 20% 4V X5R 0201 ROOM=SOC
C1481 4UF 20% 4V X5R 0201 ROOM=SOC

VDD12_PLL_DDR* Total: 1.14V - 1.26V @ 7mA MAX
PP1V2_SOC

VDD12_PLL_DDR0 AG5
VDD12_PLL_DDR1 AK29
VDD12_PLL_DDR2 D6
VDD12_PLL_DDR3 N30

1.8V @ 75mA MAX (GRP*)
1.8V @ 25mA MAX (MTR)
PP1V8_EXT_SW1

C1410 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC
C1411 4UF 20% 4V X5R 0201 ROOM=SOC
C1412 4UF 20% 4V X5R 0201 ROOM=SOC
C1413 4UF 20% 4V X5R 0201 ROOM=SOC

GRP2 IS AOP

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VDDIO18_GRP1
VDDIO18_GRP3
VDDIO18_GRP4
VDDIO18_MTR

1.8V @ 3mA MAX (CPU)
1.8V @ 0.5mA MAX (GPU)
1.8V @ 0.5mA MAX (ANE)
1.8V @ 0.3mA MAX (AMUX)
1.8V @ 1.5mA MAX (SOC)
1.8V @ 1mA MAX (FMON)
1.8V @ 0.03mA MAX (ULPPLL)
PP1V8_EXT_SW1

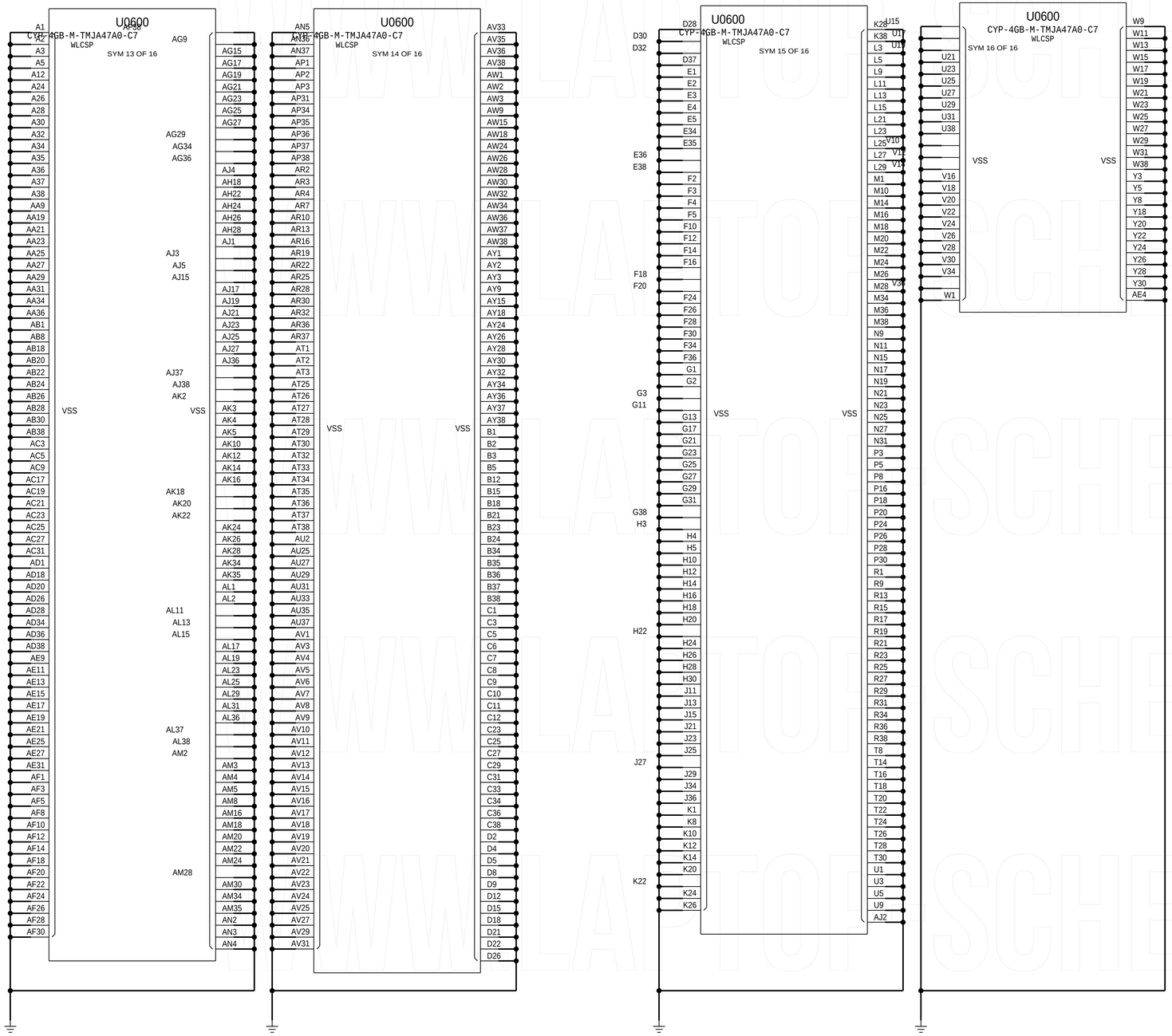
VDD18_TSADC_CPU0 P14
VDD18_TSADC_CPU1 AF16
VDD18_TSADC_CPU2 AA17
VDD18_TSADC_CPU3 AE8
VDD18_TSADC_CPU4 U14
VDD18_TSADC_CPU5 N13
VDD18_TSADC_GPU0 G15
VDD18_TSADC_ANE AL14
VDD18_AMUX AJ34
VDD18_EFUSE1 R8
VDD18_EFUSE2 AC30
VDD18_TSADC_SOC0 AE29
VDD18_TSADC_SOC1 D34
VDD18_TSADC_SOC2 M9
VDD18_FMON AC29 → PP1V8_FMON_R
VDD18_ULPPLL AL21 → PP1V8_ULPPLL_R

R1401 49.9 1% MF 1/32W 01005 ROOM=SOC → PP1V8_EXT_SW1
R1402 100 5% MF 1/32W 01005 ROOM=SOC → PP1V8_S2

C1471 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1444 4UF 20% 4V X5R 0201 ROOM=SOC

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
SOC: POWER (2/3)

SOC - POWER SUPPLIES



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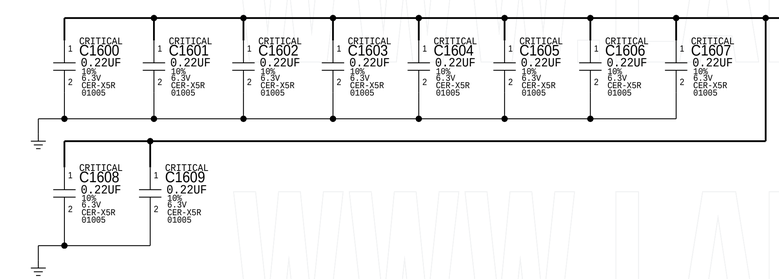
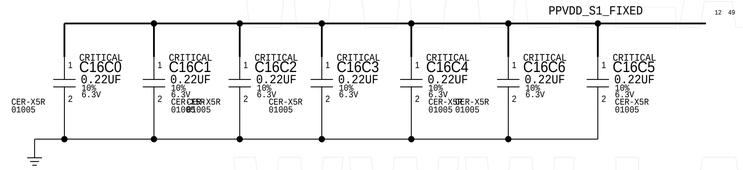
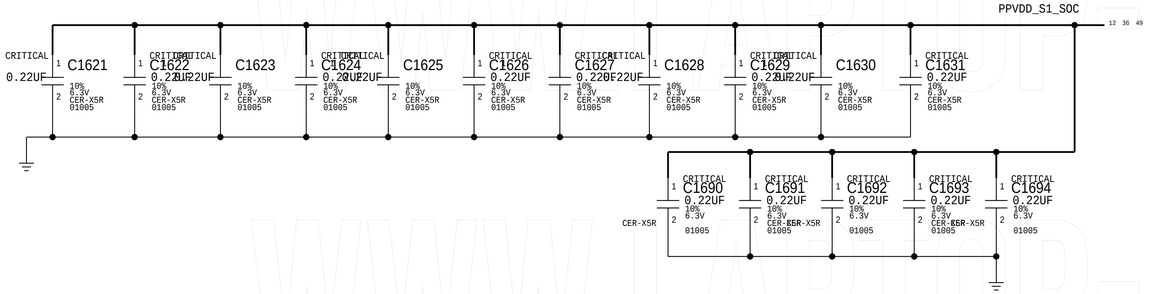
SOC: POWER (3/3)

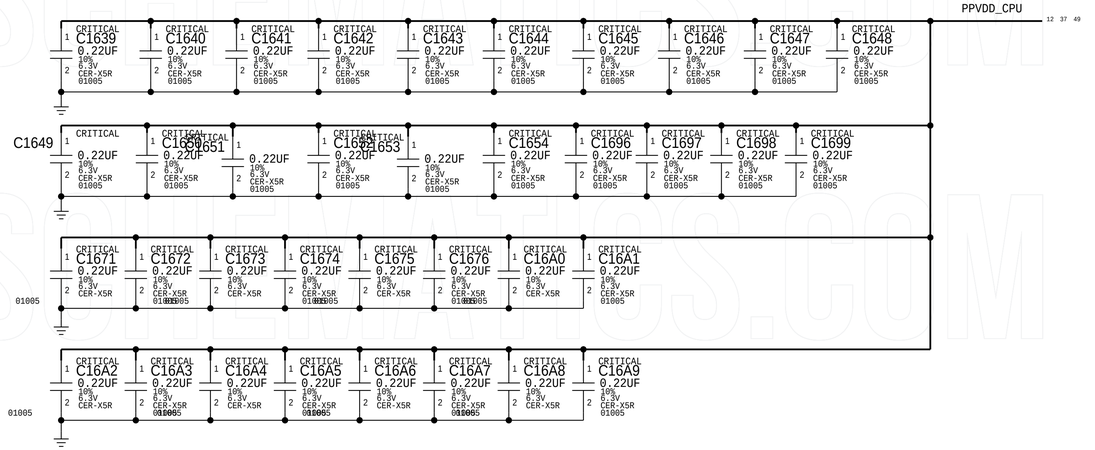
BOTTOM SIDE SOC CAPS

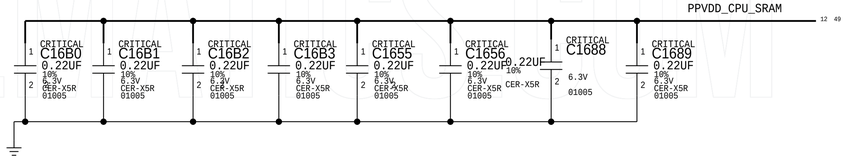
0.1UF = 132S00238 (0201, 0.11MM)

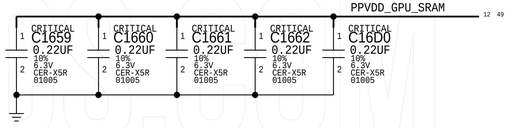


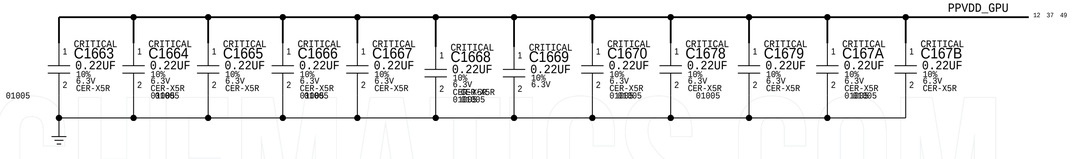


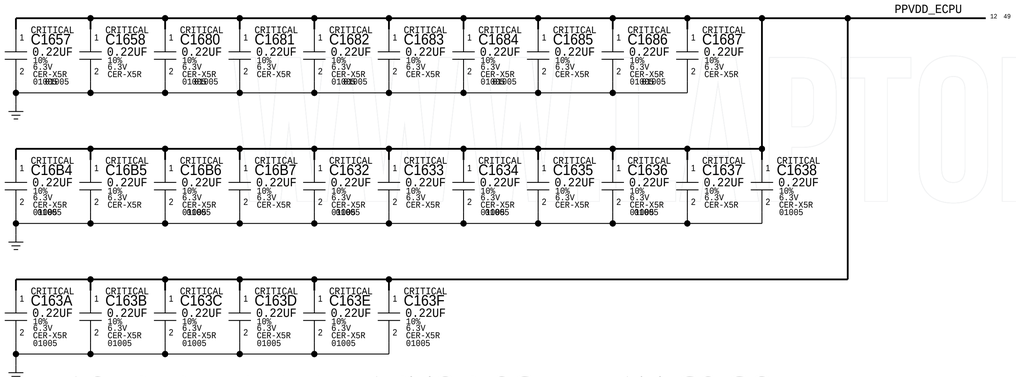












SYNC_MASTER=J21I_MLB_B SYNC_DATE=10/01/2018

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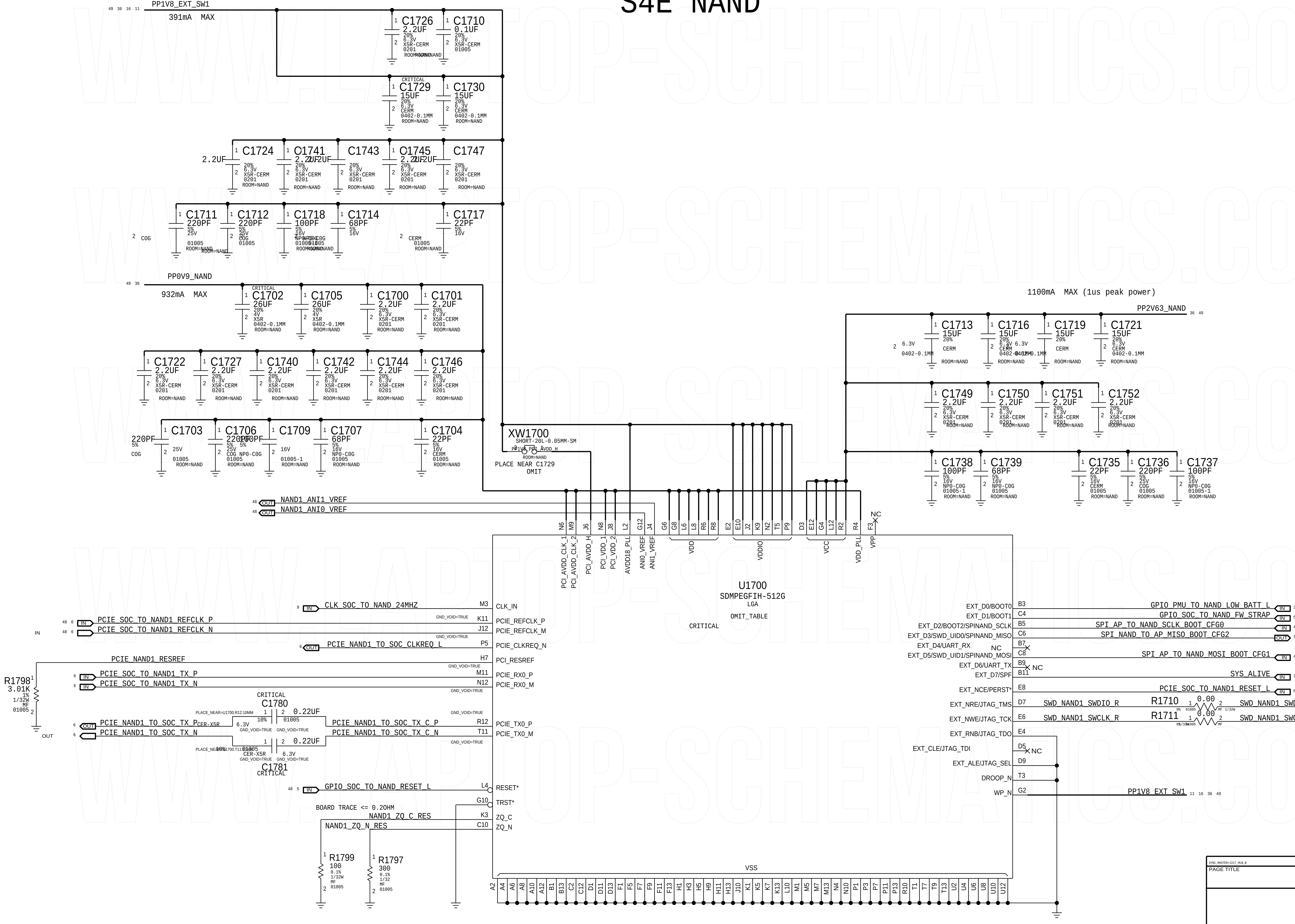
SOC: BOTTOM SIDE DECAPS

S4E NAND



SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

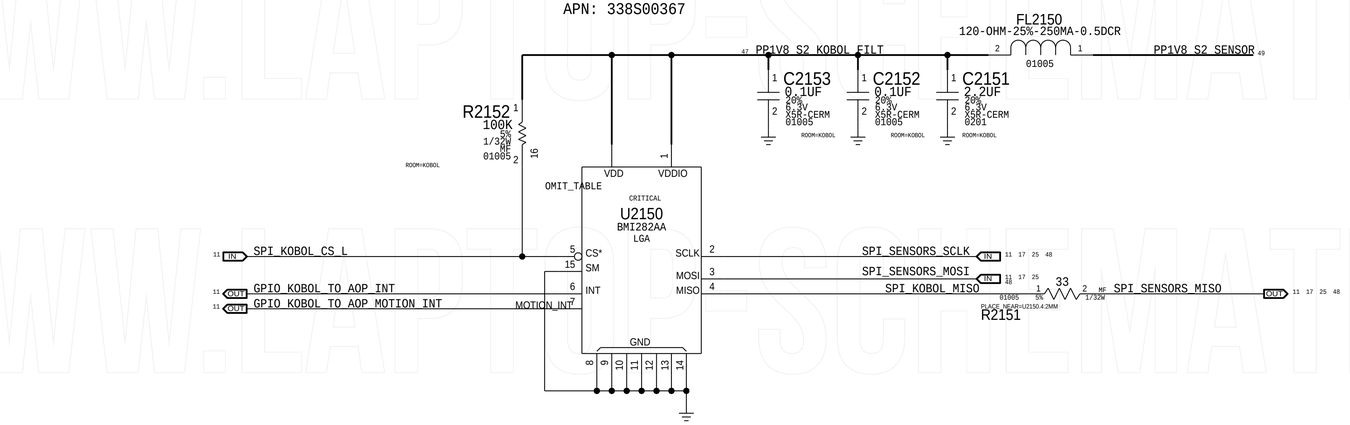
NAND: S4E NAND

SENSORS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00016	155S0686		FL2120,ECT	RDAR://PROBLEM/15809407

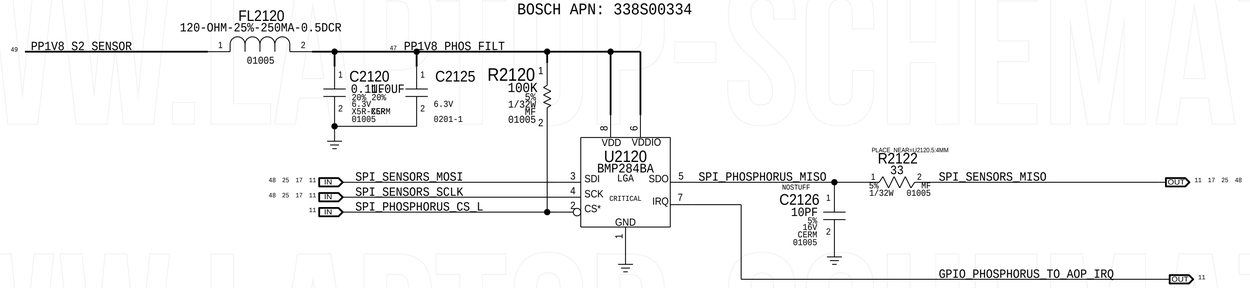
KOBOL - ACCEL & GYRO

APN: 338S00367



PHOSPHORUS2

BOSCH APN: 338S00334



PAGE TITLE

SENSOR: KOBOL, PHOS2

KONA MASTER

MARKED AS CRITICAL DUE TO PART ISSUES IN THE PAST W/0201

U2200 BCM15900B0K BGA SYM 1 OF 2 — CRITICAL

E11	AUXADC_REF		
G12	AUXBUF_AIO_INPUT_3V		
F13	AUXBUF_AIO_OUTPUT		
D10	GPIO_ADC_00	PAD_I_TOUCH0	J5
D12	GPIO_ADC_01	PAD_I_TOUCH1	H3
D11	GPIO_ADC_02	PAD_I_TOUCH2	J2
F12	GPIO_ADC_03	PAD_I_TOUCH3	J3
E10	GPIO_ADC_04	PAD_I_TOUCH4	J4
F10	GPIO_ADC_05	PAD_I_TOUCH5	K5
G10	GPIO_ADC_06	PAD_I_TOUCH6	K4
G9	GPIO_ADC_07	PAD_I_TOUCH7	K3
F8	GPIO_08	PAD_I_TOUCH8	M5
H11	GPIO_09	PAD_I_TOUCH9	L5
J9	GPIO_10	PAD_I_TOUCH10	M1
H9	GPIO_11	PAD_I_TOUCH11	K1
F7	GPIO_12	PAD_I_TOUCH12	L6
J10	GPIO_13	PAD_I_TOUCH13	N1
A6	GPIO_14	PAD_I_TOUCH14	P6
C6	GPIO_15	PAD_I_TOUCH15	N6
D9	GPIO_16	PAD_I_TOUCH16	R7
E8	GPIO_17	PAD_I_TOUCH17	N7
C9	GPIO_18	PAD_I_TOUCH18	R8
C5	GPIO_19	PAD_I_TOUCH19	M6
A7	H_INT*	PAD_I_TOUCH20	P7
A8	H_SCLK	PAD_I_TOUCH21	M7
A9	H_SDI	PAD_I_TOUCH22	N9
B8	H_SDO	PAD_I_TOUCH23	P9
B6	H_CS*	PAD_I_TOUCH24	M9
B5	H_ALT_CS*	PAD_I_TOUCH25	R9
A5	I2C_SCL	PAD_I_TOUCH26	N10
A4	I2C_SDA	PAD_I_TOUCH27	M10
A12	KMSI_MISO	PAD_I_TOUCH28	R10
B13	KMSI_MOSI	PAD_I_TOUCH29	P10
B12	KMSI_STRB_IN	PAD_I_TOUCH30	D2
A13	KMSI_STRB_OUT	PAD_I_TOUCH31	D1
C14	PSE_SYNC	PAD_I_TOUCH32	C2
B14	BOOST_ATEST	PAD_I_TOUCH33	C1
A15	BOOST_FBIN	PAD_I_TOUCH34	B1
B15	BOOST_ISENSE	PAD_I_TOUCH35	P3
D13	BOOST_NGATE	PAD_I_TOUCH36	N2
C15	BOOST_VBAT	PAD_I_TOUCH37	P1
D14	BOOST_VBAT_EN	PAD_I_TOUCH38	P2
E9	JTAG_RTCK	PAD_I_TOUCH39	P4
J7	JTAG_TCK	PAD_I_TOUCH40	G3
E7	JTAG_TMS	PAD_I_TOUCH41	D4
G7	JTAG_TDI	PAD_I_TOUCH42	D3
H8	JTAG_TDO	PAD_I_TOUCH43	G4
G6	JTAG_TRST*	PAD_I_TOUCH44	E4
C7	JTAG_SRST*	PAD_I_TOUCH45	E3
H7	RESET*	PAD_I_TOUCH46	F1
K9	TEST_MODE	PAD_I_TOUCH47	F4
K7	BOOT_CFG_0	PAD_I_TOUCH48	F3
J8	BOOT_CFG_1	PAD_I_TOUCH49	H5
R5	AFE_IO_BGBIAS	PAD_I_TOUCH50	F2
J15	XTALN	PAD_I_TOUCH51	G2
K15	XTALP	PAD_I_TOUCH52	G1
J13	XTAL_O_CLK_EXT	PAD_I_TOUCH53	H1
B4	IFO_CLK_EXT	PAD_I_TOUCH54	P11
N5	NC	PAD_I_TOUCH55	N15
N4	NC	PAD_I_TOUCH56	N12
C11	NC	PAD_I_TOUCH57	P13
		PAD_I_TOUCH58	P12
		PAD_I_TOUCH59	R12
		PAD_I_TOUCH60	N13
		PAD_I_TOUCH61	M12
		PAD_I_TOUCH62	R13
		PAD_I_TOUCH63	L13
		PAD_I_TOUCH64	P14
		PAD_I_TOUCH65	M14
		PAD_I_TOUCH66	M13
		PAD_I_TOUCH67	N14
		PAD_I_TOUCH68	M15
		PAD_I_TOUCH69	R14

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GRAPE_RX<20>	20		
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GRAPE_TX<38>	20		
GRAPE_TX<39>	20		

U2200 BCM15900B0K BGA SYM 2 OF 2 — CRITICAL

B3	AFE_I_VDDHV15_EXT	AUXBUF_AVSS	F14
C4	AFE_I_VDDHV15_EXT	AUXADC_AVSS	C10
L7	AFE_I_VDDHV15_EXT	VSS	D6
E5	AFE_I_VDDHV15_EXT	VSS	D8
M11	AFE_I_VDDHV15_EXT	VSS	F6
H2	AFE_I_VDDHV15_EXT	VSS	
K6	AFE_I_VDDHV15_EXT	VSS	F9
L1	AFE_I_VDDHV15_EXT	VSS	G8
L9	AFE_I_VDDHV15_EXT	VSS	H10
M3	AFE_I_VDDHV15_EXT	VSS	K8
E2	AFE_I_VDDHV15_EXT	VSS	A14
N3	AFE_I_VDDHV15_EXT	VSS	E14
L12	AFE_I_VDDHV15_EXT	VSS	A1
G5	AFE_I_VDDHV15_EXT	VSS	A3
R15	AFE_I_VDDHV15_EXT	VSS	B7
E13	BOOST_VDDA	VSS	H12
C12	OTP_TMON_I_VDDA_3P3_EXT	VSS	H13
R1	AFE_PMU_I_VDDA_3P3_EXT	VSS	K11
G13	AUXBUF_PMU_I_VDDA_3P3_EXT	VSS	K12
G14	AUXBUF_PMU_I_VDDHV_AUX_EXT	VSS	K13
G15	AUXBUF_PMU_O_VDD_AUX_CAP	VSS	D15
C3	AFE_I_VDDANA_3P3_AFE_PMU	VSS	E15
D5	AFE_I_VDDANA_3P3_AFE_PMU	VSS	F15
H6	AFE_I_VDDANA_3P3_AFE_PMU	VSS	G11
L4	AFE_I_VDDANA_3P3_AFE_PMU	J11	
L3	AFE_I_VDDANA_3P3_AFE_PMU	J12	
L8	AFE_I_VDDANA_3P3_AFE_PMU	VSS	K10
M2	AFE_I_VDDANA_3P3_AFE_PMU	XTAL_AVSS	H15
R11	AFE_I_VDDANA_3P3_AFE_PMU	XTAL_AVSS	K14
M8	AFE_I_VDDANA_3P3_AFE_PMU	CORE_PMU_I_AVSS	B10
N8	AFE_I_VDDANA_3P3_AFE_PMU	AUXBUF_PMU_I_AVSS	H14
J6	AFE_I_VDDANA_3P3_AFE_PMU	PAD_I_AVSS	P9
L11	AFE_I_VDDANA_3P3_AFE_PMU	PAD_I_AVSS	E1
L14	AFE_I_VDDANA_3P3_AFE_PMU	PAD_I_AVSS	J1
R6	AFE_PMU_O_VDDANA_3P3_PMU	PAD_I_AVSS	N11
R2	AFE_PMU_O_AVDD1P2_CAP	PAD_I_AVSS	L2
R4	AFE_PMU_O_AVDD1P2_CAP	PAD_I_AVSS	P15
J14	XTAL_PLL_AVDD1P8_I_VDDLDO_1P8_EXT	PAD_I_AVSS	K2
F11	AUXADC_AVDDC_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	L10
E12	AUXADC_AVDD_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	L15
R3	AFE_PMU_I_VDDLDO_1P8_EXT	PAD_I_AVSS	M16
B9	AON_PAD_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	P7
D7	AON_PAD_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	P5
E6	AON_PAD_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	P8
A2	I2C_PAD_I_VDDIO_1P8_3P3_EXT	PAD_I_AVSS	H4
C13	CORE_PAD_I_VDDIO_1P8_3P3_EXT		
C8	CORE_PAD_I_VDDIO_1P8_3P3_EXT		
B11	CORE_PMU_I_AON_VDDIO_1P8_3P3_EXT		
A10	CORE_PMU_I_VDDLDO_1P8_EXT		
A11	CORE_PMU_O_VDDCORE_1P2_CAP		

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
	138S0700	C2206,ETC	RDAR://PROBLEM/23618071	
376S00191	376S00061		Q2202	

371S00118	371S00175		D2201
371S00117	371S00175		D2201

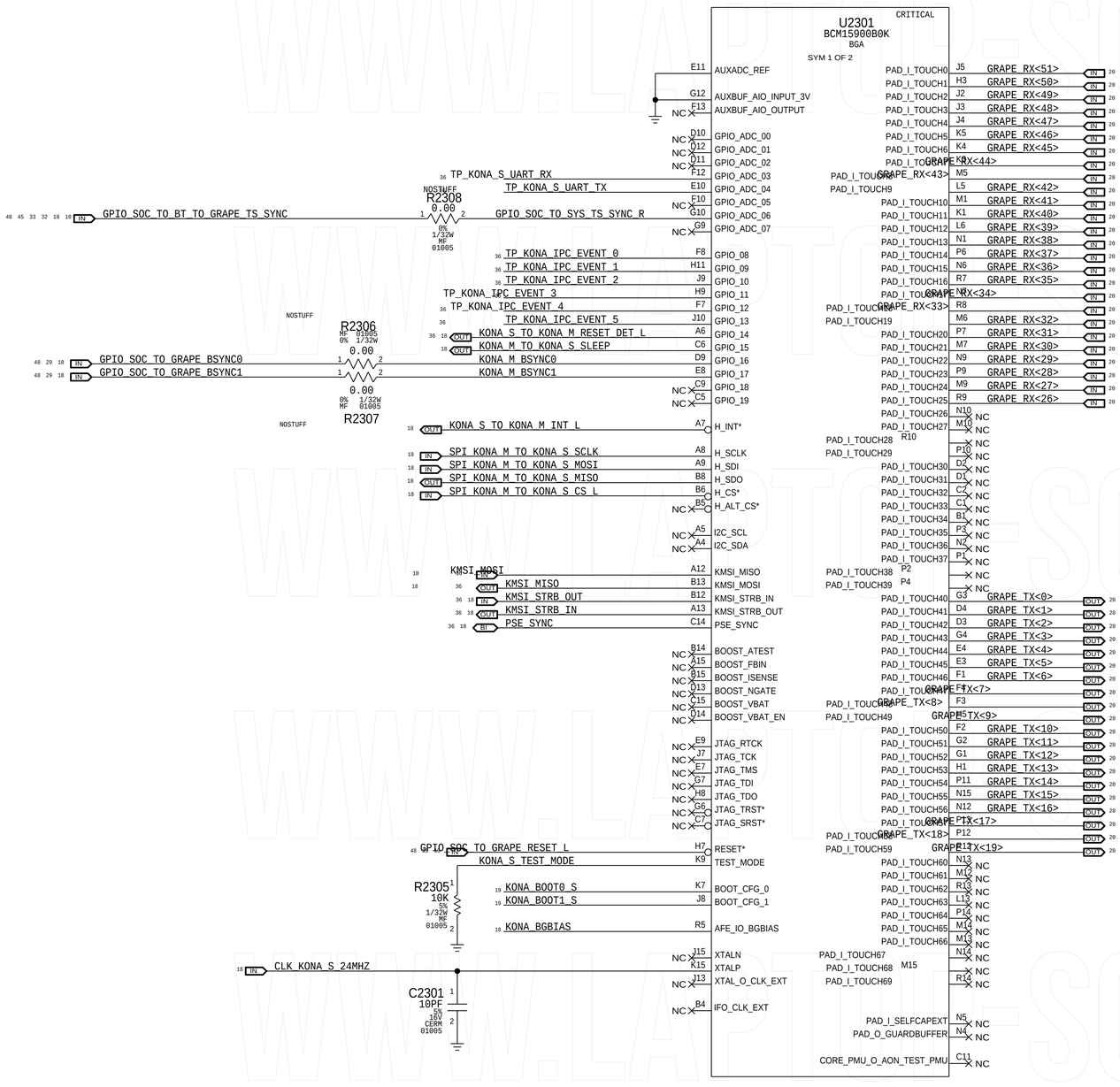
BOOT OPTION

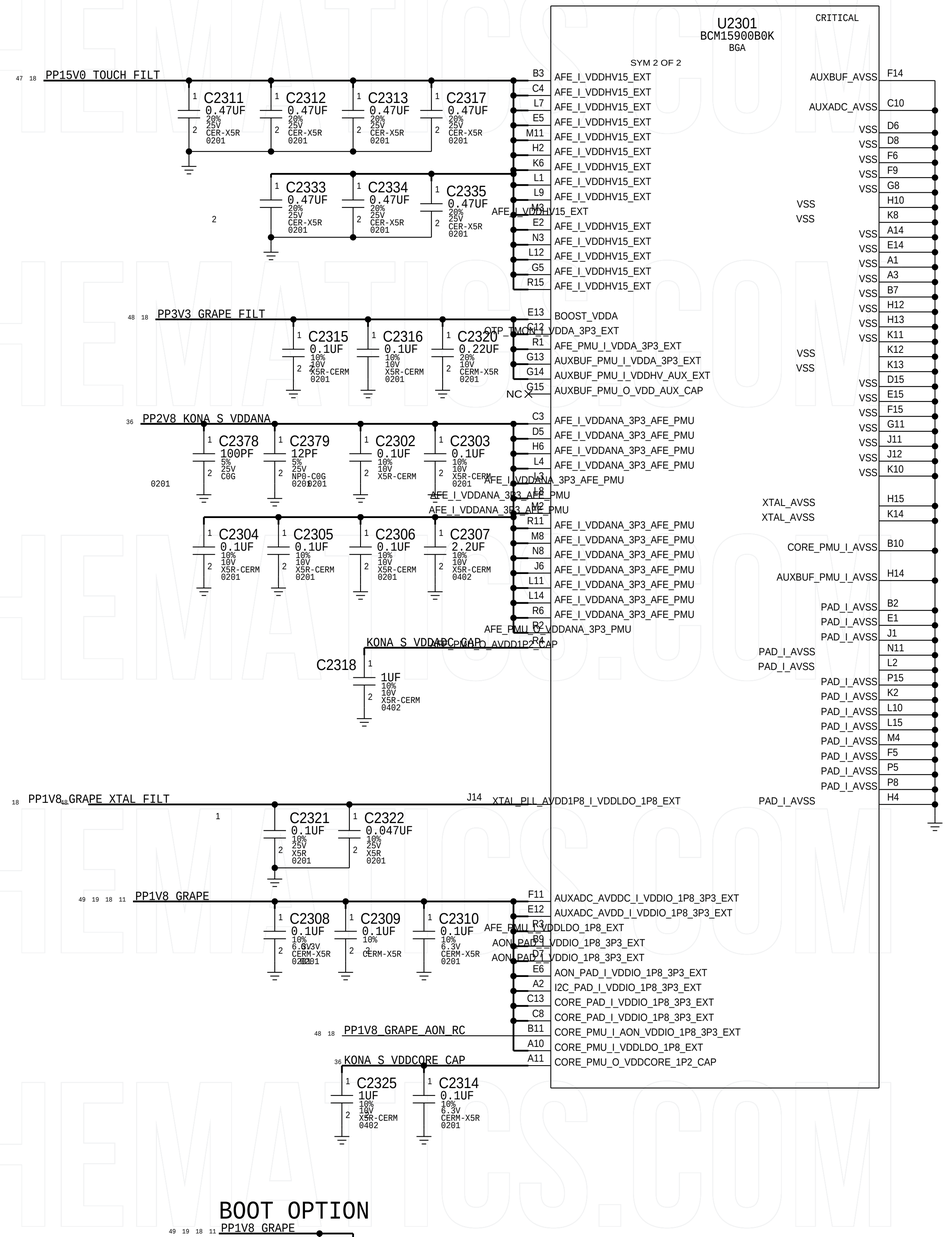
15V BOOST

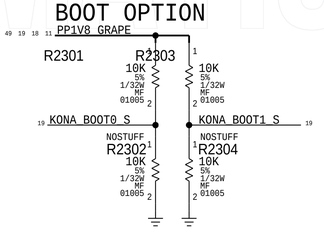
RELEASED BY WWW.LAPTOP-SCHEMATICS.COM

SYNC_MASTER=J217_MLB_B	SYNC_DATE=10/01/2018
PAGE TITLE	TOUCH: KONA MASTER

KONA: SLAVE







SYNC_MASTER=J217_MLB_B	SYNC_DATE=10/01/2018
PAGE TITLE	TOUCH: KONA SLAVE

TOUCH FLEX CONNECTOR (SENSE)

MATCHES J207_GRAPE_FLEX 051-01606_3.0.0

MLB: 516S00063
FLEX: 516S00064

MOUNTING PINS CAN BE USED FOR ELECTRICAL CONNECTIONS

J2400
505066-5422
F-ST-SM

	GRAPE_RX<0>	1	2	GRAPE_RX<26>	OUT	18	19
18 OUT	GRAPE_RX<1>	3	4	GRAPE_RX<27>	OUT	18	19
18 OUT	GRAPE_RX<2>	5	6	GRAPE_RX<28>	OUT	18	19
18 OUT	GRAPE_RX<3>	7	8	GRAPE_RX<29>	OUT	18	19
18 OUT	GRAPE_RX<4>	9	10	GRAPE_RX<30>	OUT	18	19
18 OUT	GRAPE_RX<5>	11	12	GRAPE_RX<31>	OUT	18	19
18 OUT	GRAPE_RX<6>	13	14	GRAPE_RX<32>	OUT	18	19
18 OUT	GRAPE_RX<7>	15	16	GRAPE_RX<33>	OUT	18	19
OUT 18	GRAPE_RX<8>	17	18	GRAPE_RX<34>	OUT	18	19
18 OUT	GRAPE_RX<9>	19	20	GRAPE_RX<35>	OUT	18	19
OUT 18	GRAPE_RX<10>	21	22	GRAPE_RX<36>	OUT	18	19
18 OUT	GRAPE_RX<11>	23	24	GRAPE_RX<37>	OUT	18	19
18 OUT	GRAPE_RX<12>	25	26	GRAPE_RX<38>	OUT	18	19
18 OUT	GRAPE_RX<13>	27	28	GRAPE_RX<39>	OUT	18	19
18 OUT	GRAPE_RX<14>	29	30	GRAPE_RX<40>	OUT	18	19
18 OUT	GRAPE_RX<15>	31	32	GRAPE_RX<41>	OUT	18	19
18 OUT	GRAPE_RX<16>	33	34	GRAPE_RX<42>	OUT	18	19
18 OUT	GRAPE_RX<17>	35	36	GRAPE_RX<43>	OUT	18	19
OUT 18	GRAPE_RX<18>	37	38	GRAPE_RX<44>	OUT	18	19
18 OUT	GRAPE_RX<19>	39	40	GRAPE_RX<45>	OUT	18	19
OUT 18	GRAPE_RX<20>	41	42	GRAPE_RX<46>	OUT	18	19
18 OUT	GRAPE_RX<21>	43	44	GRAPE_RX<47>	OUT	18	19
18 OUT	GRAPE_RX<22>	45	46	GRAPE_RX<48>	OUT	18	19
18 OUT	GRAPE_RX<23>	47	48	GRAPE_RX<49>	OUT	18	19
18 OUT	GRAPE_RX<24>	49	50	GRAPE_RX<50>	OUT	18	19
18 OUT	GRAPE_RX<25>	51	52	GRAPE_RX<51>	OUT	18	19
		53	54				
		57	58				

55 56

TOUCH FLEX CONNECTOR (DRIVE)

MATCHES J207_GRAPE_FLEX 051-01606_3.0.0

MLB: 516S00224
FLEX: 516S00225

MOUNTING PINS CAN BE USED FOR ELECTRICAL CONNECTIONS

J2401
505066-4222
F-ST-SM

18	GRAPE_TX<20>	1	2	GRAPE_TX<0>	IN	18	19
18 IN	GRAPE_TX<21>	3	4	GRAPE_TX<1>	IN	18	19
18 IN	GRAPE_TX<22>	5	6	GRAPE_TX<2>	IN	18	19
18 IN	GRAPE_TX<23>	7	8	GRAPE_TX<3>	IN	18	19
18 IN	GRAPE_TX<24>	9	10	GRAPE_TX<4>	IN	18	19
18 IN	GRAPE_TX<25>	11	12	GRAPE_TX<5>	IN	18	19
18 IN	GRAPE_TX<26>	13	14	GRAPE_TX<6>	IN	18	19
18 IN	GRAPE_TX<27>	15	16	GRAPE_TX<7>	IN	18	19
18 IN	GRAPE_TX<28>	17	18	GRAPE_TX<8>		18	19
IN 18	GRAPE_TX<29>	19	20	GRAPE_TX<9>		18	19
18 IN	GRAPE_TX<30>	21	22	GRAPE_TX<10>		18	19
18 IN	GRAPE_TX<31>	23	24	GRAPE_TX<11>	IN	18	19
18 IN	GRAPE_TX<32>	25	26	GRAPE_TX<12>	IN	18	19
18 IN	GRAPE_TX<33>	27	28	GRAPE_TX<13>	IN	18	19
18 IN	GRAPE_TX<34>	29	30	GRAPE_TX<14>	IN	18	19
18 IN	GRAPE_TX<35>	31	32	GRAPE_TX<15>	IN	18	19
18 IN	GRAPE_TX<36>	33	34	GRAPE_TX<16>	IN	18	19
18 IN	GRAPE_TX<37>	35	36	GRAPE_TX<17>	IN	18	19
18	GRAPE_TX<38>	37	38	GRAPE_TX<18>		18	19
IN 18	GRAPE_TX<39>	39	40	GRAPE_TX<19>		18	19
		4241					
		45	46				

44 43

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018

PAGE TITLE

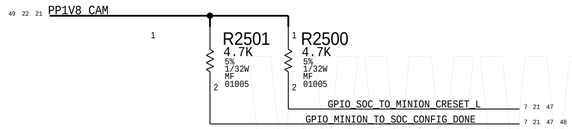
TOUCH: GRAPE CONN

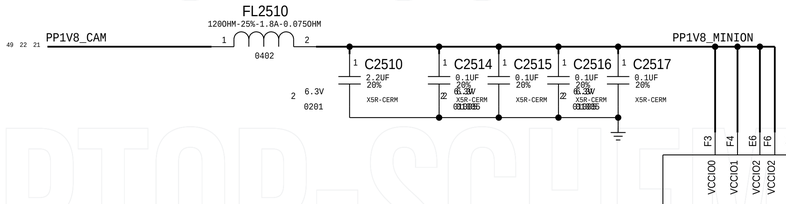
MINION

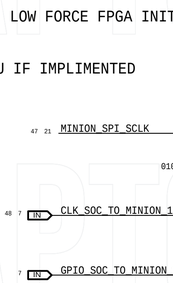
VCCIO: NOM 1.8V
VCC: NOM 1.2V (1.25V CAMERA RAIL IS ACCEPTABLE)
VCCAUX: NOM 2.5V (2.6V CAMERA RAIL IS ACCEPTABLE)

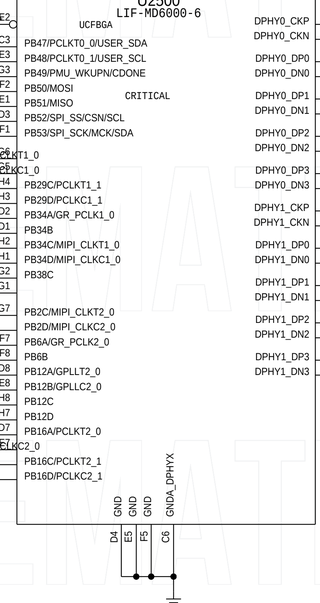
LOW FORCE FPGA INITIALIZE

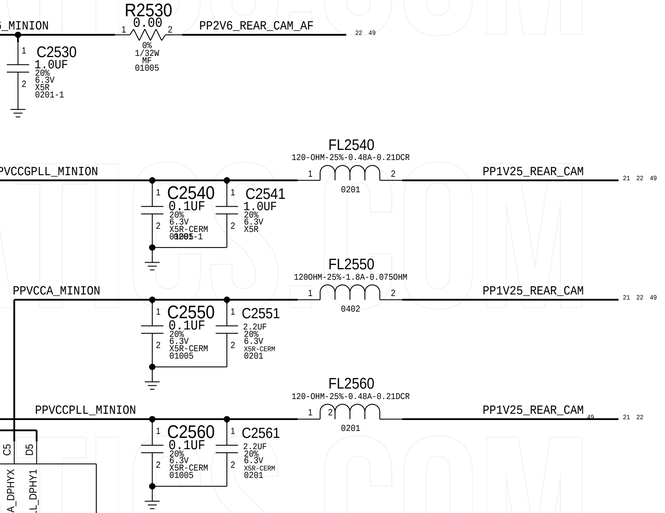
HIGH INDICATES FPGA INITIALIZED AND LOW WAKE PMU IF IMPLIMENTED

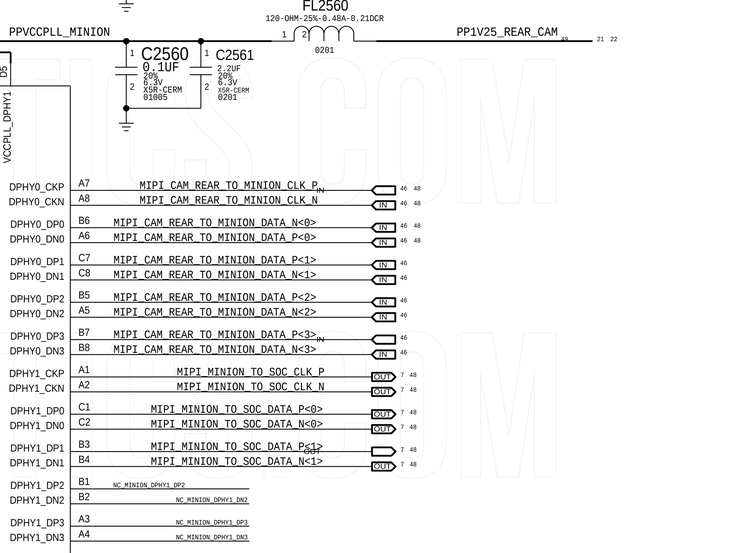


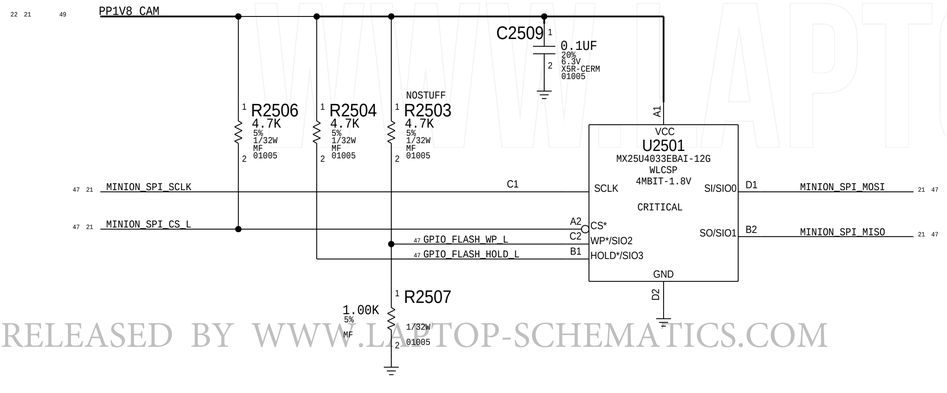






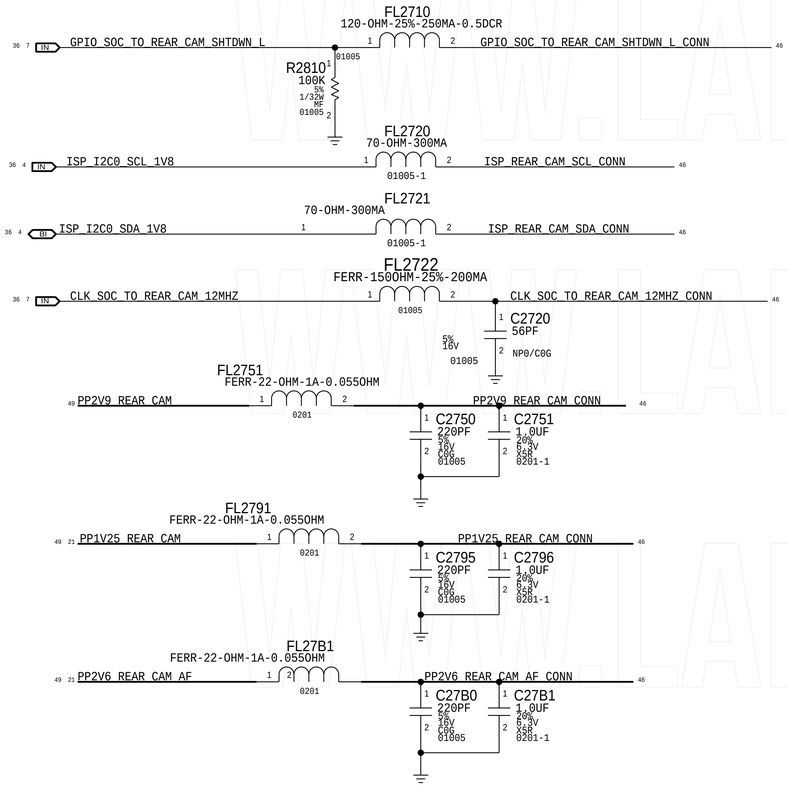




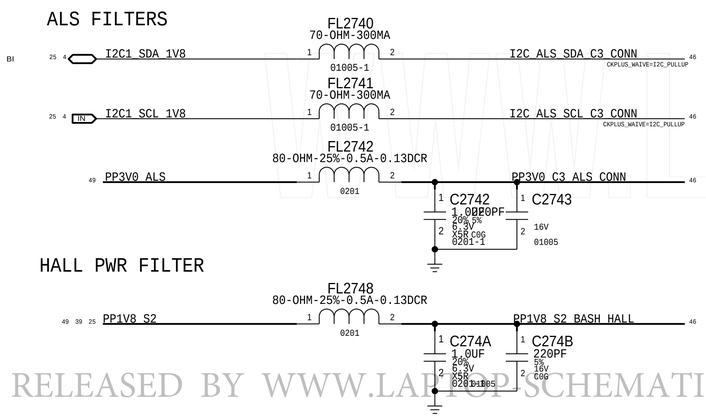


SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018
PAGE TITLE
CAMERA: MIPI BRIDGE

CORNER3 XFER FLEX B2B

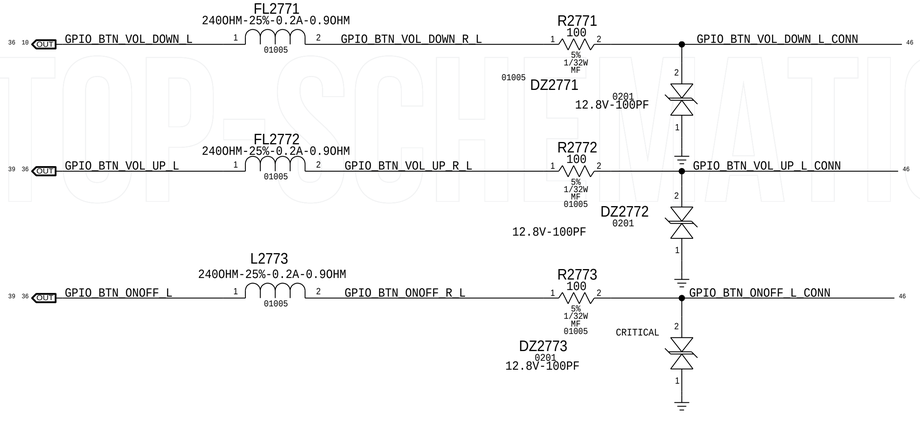


ALS FILTERS



HALL PWR FILTER

BUTTON FILTERS/ESD



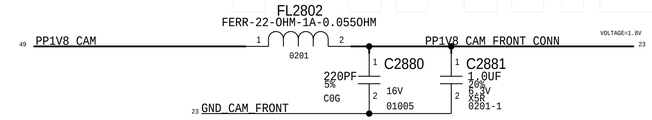
SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018

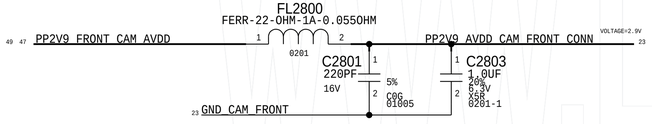
PAGE TITLE

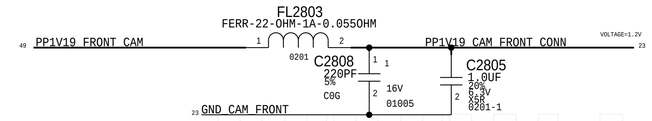
FLEX CONNS: CORNER 3

FRONT CAMERA (NH)

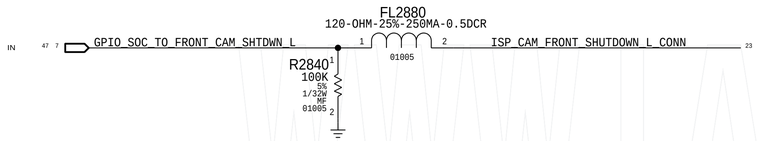
POWER FILTERS

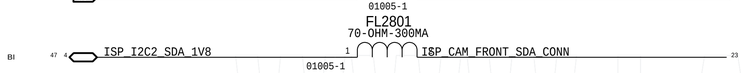


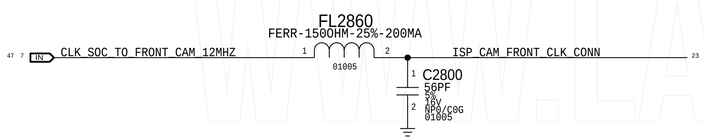




IO FILTERS





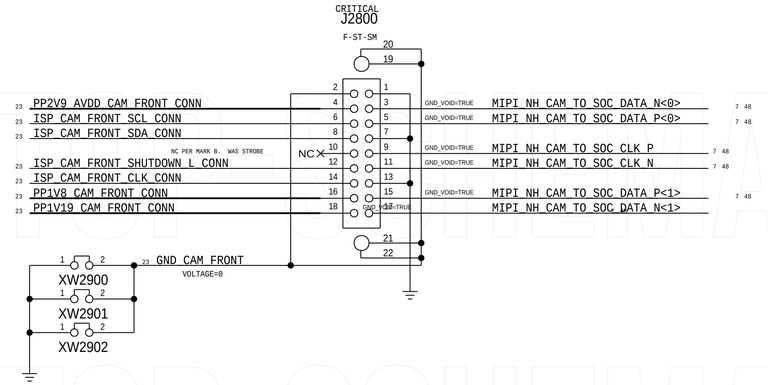


FRONT CAMERA CONNECTOR

MATCHES J120_FRONT_CAM_FLEX_051-01272_2.0.0

FLEX SIDE: 516S00194

MLB SIDE: 516S00193



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

SYNC_MASTER=2017_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

CAMERA: FRONT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00338	155S00402			L3000-5

CLIFDEN

49 24 PP1V8_S2_EXT_SW2
R3098 10K 5% 1/32W MF 01005
R3099 10K 5% 1/32W MF 01005
24 9 GPIO_SOC_TO_BELFIELD_RESET_L
24 10 GPIO_SOC_TO_CODEC_RESET_L

49 PP1V7_S2_VA_VCP
C3001 4.7UF 20% 6.3V X5R 402-2201
C3003 0.1UF 10% CERM-X5R
C3009 2.2UF 20% 6.3V X5R-CERM 0201
CRITICAL C3008 4.7UF 20% 6.3V X5R 402
CRITICAL C3007 4.7UF 20% 6.3V X5R 402
L83_PVCP
L83_NVCP
CRITICAL C3051 2.2UF 20% 6.3V X5R-CERM 0201
24 GND_AUDIO_CODEC

PLACE_NEAR=U3000.A3:5MM
PP1V8_S2_EXT_SW2 24 49
C3002 0.1UF 10% 6.3V X5R-CERM 01005
PPVCC_MAIN 24 49
C3004 0.1UF 10% 6.3V X5R-CERM 0402-9
CRITICAL C3040 10UF 20% CERM-X5R
CRITICAL C3041 10UF 20% 6.3V CERM-X5R 0402-9
CRITICAL C3042 10UF 20% CERM-X5R

U3000
CS42L83A
WLCSP-SKT

		E6	+VCP_FILT
		G6	-VCP_FILT
		F6	GNDCP
49 24 PPVCC_MAIN	R3019 10K 5% 1/32W MF 01005 2 VL_SEL	C4	VL_SEL
		D4	DIGLDO_PDN*
48 9 OUT GPIO_CODEC_TO_SOC_IRQ_L	B7		INT*
47 39 OUT GPIO_CODEC_TO_PMU_WAKE_L	C6		WAKE*
24 10 IN GPIO_SOC_TO_CODEC_RESET_L	C5		RESET*
NC	A6		SPDIF_TX
	D3		SWIRE_SEL
48 11 IN I2S_AOP_TO_CODEC_LRCK	B5		ASP_LRCK/FSYNC
48 11 IN I2S_AOP_TO_CODEC_DOUT	A5		SWIRE_SD/ASP_SDIN
48 11 OUT I2S_CODEC_TO_AOP_DOUT	R3011 22 5% 1/32W MF 01005	A4	ASP_SDOUT
48 11 IN I2S_AOP_TO_CODEC_BCLK	B4		SWIRE_CLK/ASP_SCLK
	C3		AD0
	B2		AD1
4 BI I2C3_SDA_1V8	A1		SDA
4 IN I2C3_SCL_1V8	A2		SCL
	E7		FLYP
	F7		FLYC
	G7		FLYN
	C1		FILT_P

CRITICAL C3005 4.7UF 20% 6.3V X5R 402 L83_FLYP
CRITICAL C3006 4.7UF 20% 6.3V X5R 402 L83_FLYC
L83_FLYN
L83_FILT
C3010 10UF 20% 6.3V CERM 0402-3
VOLTAGE=0V
24 GND_AUDIO_CODEC
GNDA GNDHS GNDD GNDL
XW3000 SM

		D5	HPSENSA
		E5	HPOUTA
		F5	HPSENSB
		G5	HPOUTB
		F1	HS4
		E2	HS_CLAMP2
		E1	HSIN+
		G2	HS3
		F2	HS_CLAMP1
		D1	HSIN-
		F4	HS4_REF
		G4	HS3_REF
		G3	RING_SENSE
NC		F3	TIP_SENSE
		F3	HSBIAS_FILT
		E3	HSBIAS_FILT_REF

CODEC_HP_LEFT
CODEC_HP_RIGHT
CODEC_HP_HS4
XW3006 SHORT-10L-0.1MM-SM NO_XNET_CONNECTION=1
CODEC_HP_HSINP
CODEC_HP_HS3
XW3007 SM NO_XNET_CONNECTION=1
CODEC_HP_HSINN
CODEC_HP_HS4_REF
CODEC_HP_HS3_REF
CODEC_HP_DET
HSBIAS_FILT
HSBIAS_FILT_REF
CRITICAL C3012 4.7UF 20% 6.3V X5R 402
R3020 3.3K 5% 1/32W MF 01005
CODEC_HP_DET_R

R3021 1.00K 5% 1/32W MF 01005
R3022 1.00K 5% 1/32W MF 01005

L3000 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_LEFT_CONN OUT 46 47
L3001 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_RIGHT_CONN OUT 46 47
L3002 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_HS4_CONN IN 46 47
L3003 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_HS3_CONN IN 46 47
RDAR//PROBLEM/26018872
L3004 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_HS4_REF_CONN IN 46 47
L3005 FERR-330HM-25%-1.5A 0201 CRITICAL — CODEC_HP_HS3_REF_CONN IN 46 47
L3020 240-OHM-0.2A-0.8-OHM 0201-2 — CODEC_HP_HEADSET_DET_CONN IN 46 47
NOSTUFF C3020 4700PF 10% 6.3V X5R 01005

BELFIELD

49 24 PPVCC_MAIN
C3062 0.1UF 10% 16V X5R-CERM 0201
PP1V8_S2_EXT_SW2 24 49
C3061 0.1UF 20% 6.3V X5R-CERM 01005

U3050
CS46L10
WLCSP
CRITICAL

		D5	VP
		B5	VD
NC		A5	VD_FILT
OUT 47 39	GPIO_BELFIELD_TO_PMU_WAKE_L	D2	WAKE*
47 9 OUT	GPIO_BELFIELD_TO_SOC_IRQ_L	D3	INT*
24 9 IN	GPIO_SOC_TO_BELFIELD_RESET_L	D4	RESET*
48 9 IN	I2S0_SOC_TO_BELFIELD_MCLK	B1	MCLK
48 9 IN	I2S0_SOC_TO_BELFIELD_BCLK	A1	SCLK
48 9 IN	I2S0_SOC_TO_BELFIELD_LRCK	B2	LRCK/FSYNC
48 9 OUT	I2S0_BELFIELD_TO_SOC_DOUT	A2	AD2/SDOUT
48 9 IN	I2S0_SOC_TO_BELFIELD_DOUT	A3	SDIN
48 9 IN	SPI_BELFIELD_CS_L	B3	AD0/CS_L
IN 9	SPI_BELFIELD_SCLK	A4	SCL/CCLK
IN 48 9	SPI_BELFIELD_MOSI	C4	AD1/MOSI
OUT 48 9	SPI_BELFIELD_MISO	B4	SDA/MISO
		C3	DIGLDO_PDN
		D1	D+
		C1	D-
		C2	MBUS_REF
		C5	GND

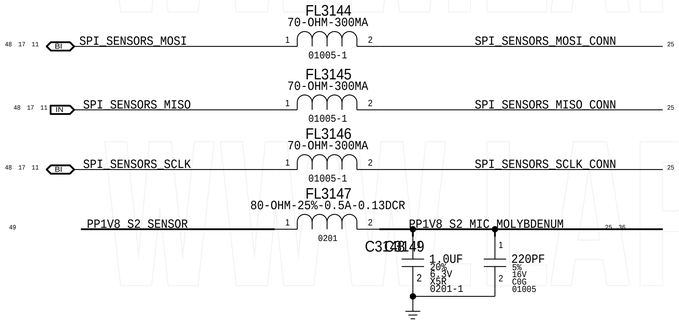
D+ D1 BELFIELD_MBUS_P
D- C1 BELFIELD_MBUS_N
MBUS_REF C2 BELFIELD_MBUS_REF IN 27

R3030 12 5% 1/20W MF 201
R3031 12 5% 1/20W MF 201
NO_XNET_CONNECTION=1
C3030 100PF 5% 16V NP0-C0G 01005-1
NOSTUFF C3031 100PF 5% 16V NP0-C0G 01005
C3032 100PF 5% 16V NP0-C0G 01005-1 NO_XNET_CONNECTION=1
MIKEY_HYDRA_P BI 27 47
MIKEY_HYDRA_N BI 27 47

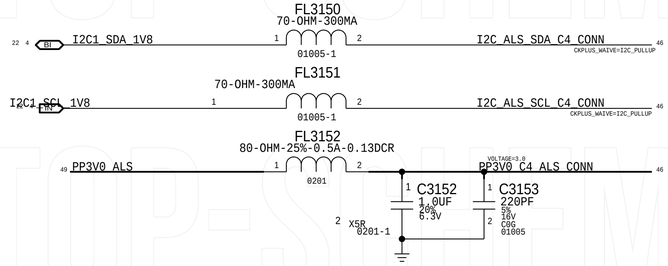
SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018
PAGE TITLE
AUDIO: CLIFDEN, BELFIELD

CORNER 4 + DMIC FLEX FILTERS

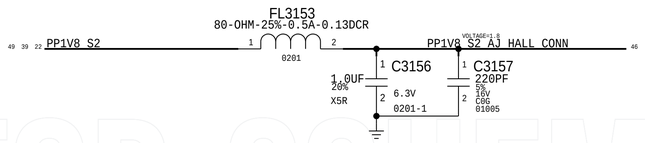
MOLYBDENUM SPI FILTERS

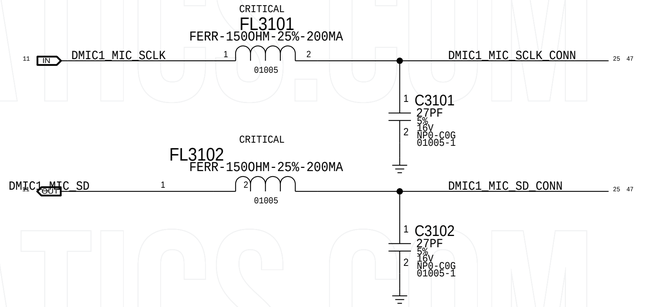


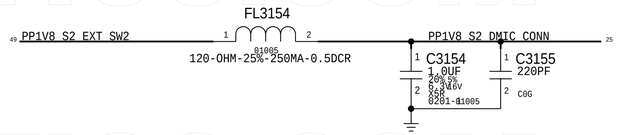
ALS FILTERS



HALL FILTER







MIC FLEX B2B

MATCHES J207_MIC_FLEX_051-01915_0.5.0

MLB APN: 516S1278

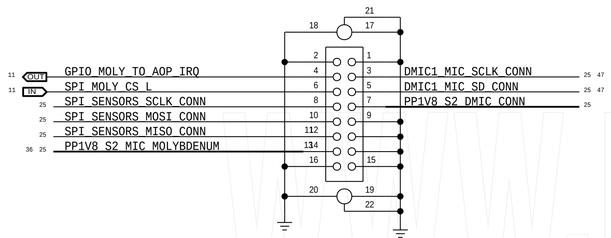
FLEX APN: 516S1280

CRITICAL

J3100

24-5857-016-201-829

F-ST-SM



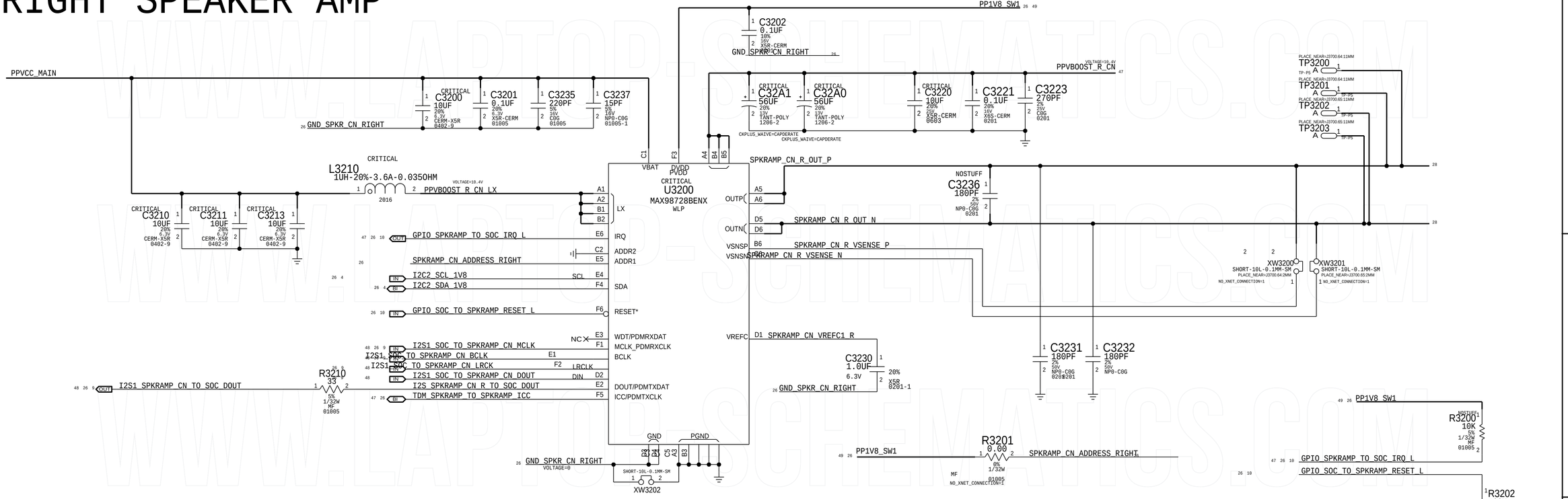
ROUTING	SELECT	LOCATION	DATA ASSERTS ON	DATA LATCHED ON
MIC1	DMIC1	HIGH	CENTER SPLINE	CLK RISING EDGE	CLK FALLING EDGE
MIC2	DMIC1	LOW	REAR	CLK FALLING EDGE	CLK RISING EDGE

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

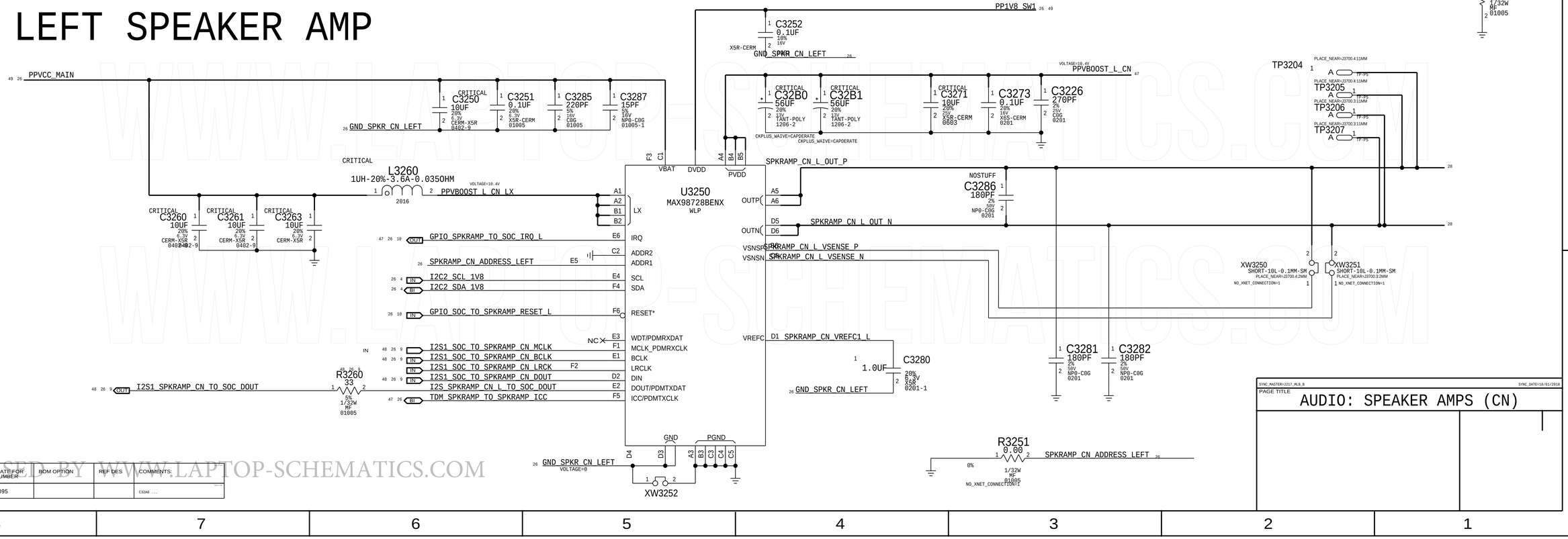
PAGE TITLE

FLEX CONNS: C4 & DMIC

CN RIGHT SPEAKER AMP



CN LEFT SPEAKER AMP



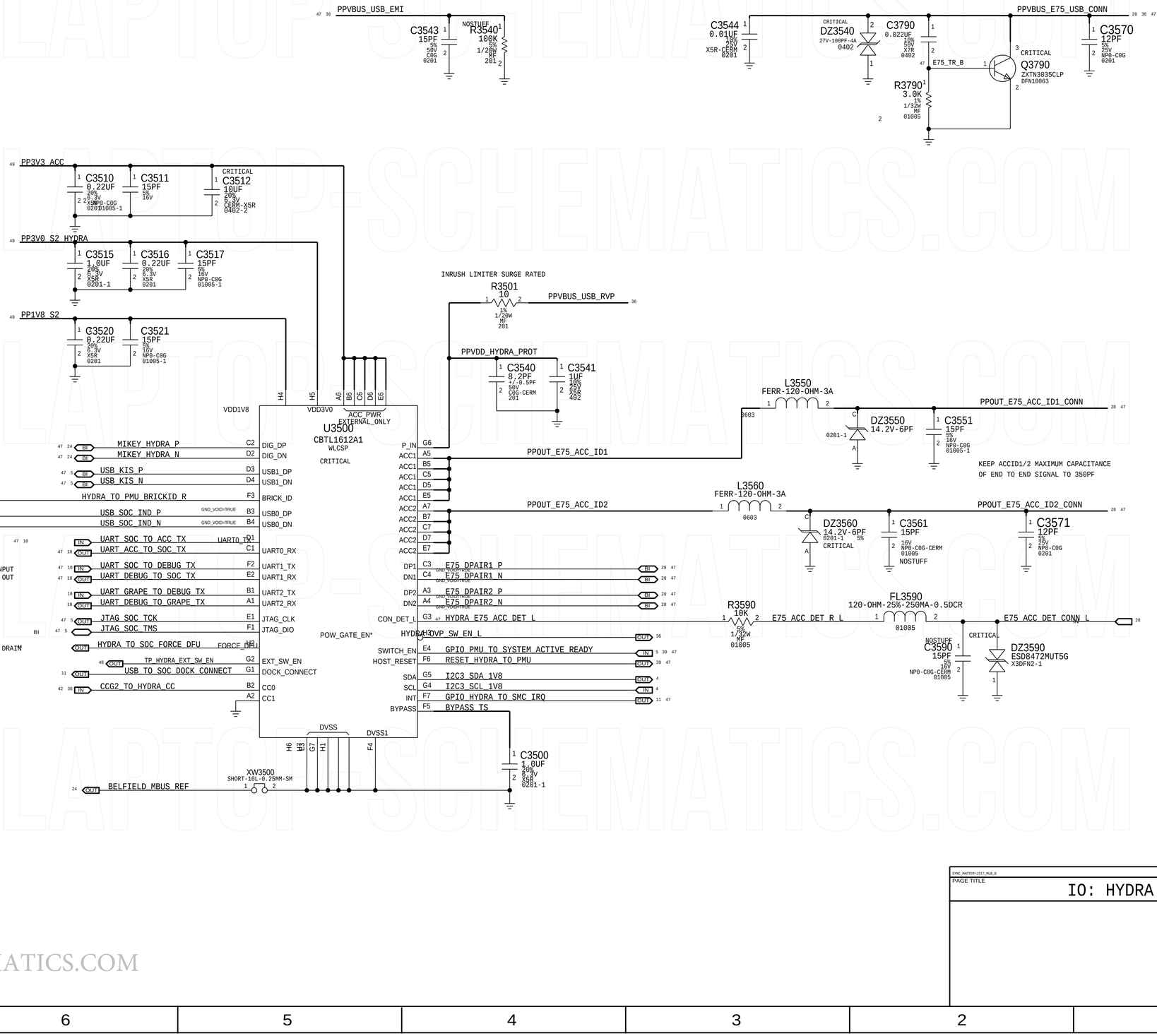
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S00073	128S00095			C32A0 ...

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

AUDIO: SPEAKER AMPS (CN)

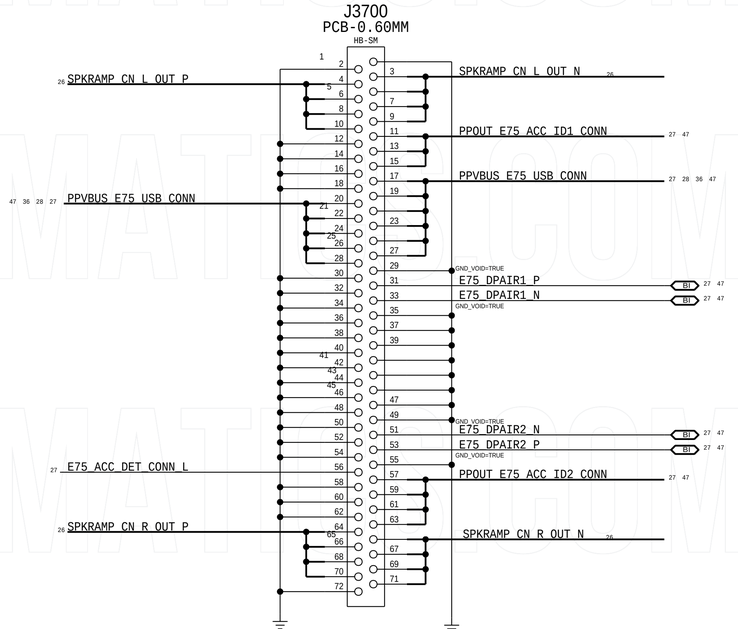
HYDRA



HOTBAR CONNECTOR TO I/0 FLEX

TO BE MATCHED TO J217_IO_FLEX

MLB APN: 998-01935
FLEX APN: 998-01936

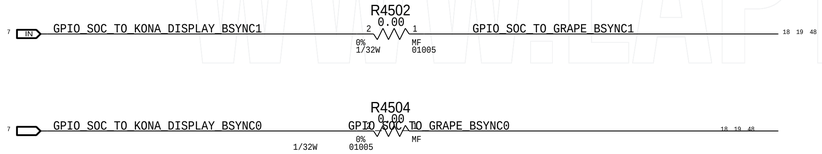


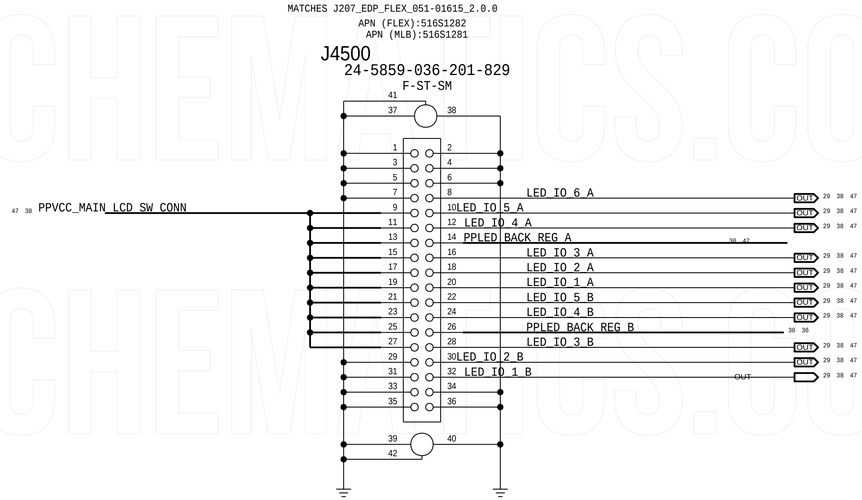
$SYNC_MASTER=J217_MLB_B $SYNC_DATE=10/01/2018

PAGE TITLE

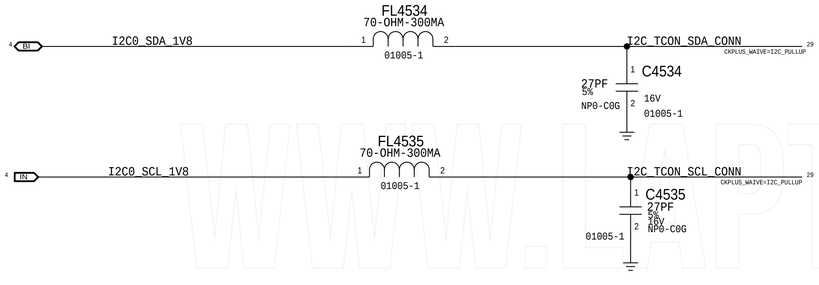
IO: HOTBAR,SIM,XBAR

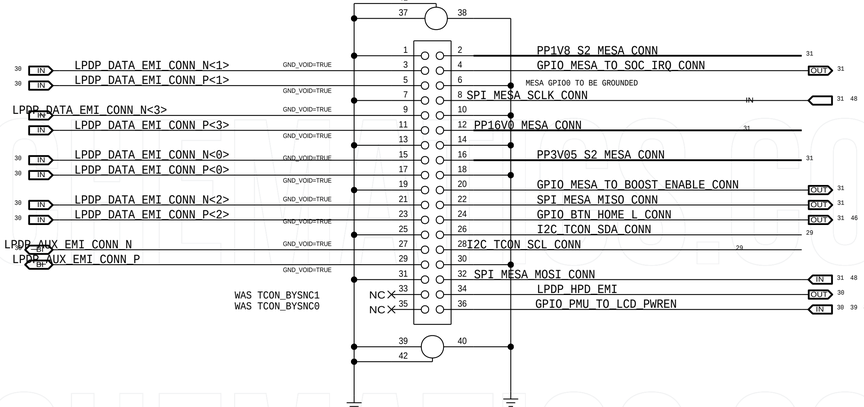
EDP FLEX FILTERS AND CONNECTORS





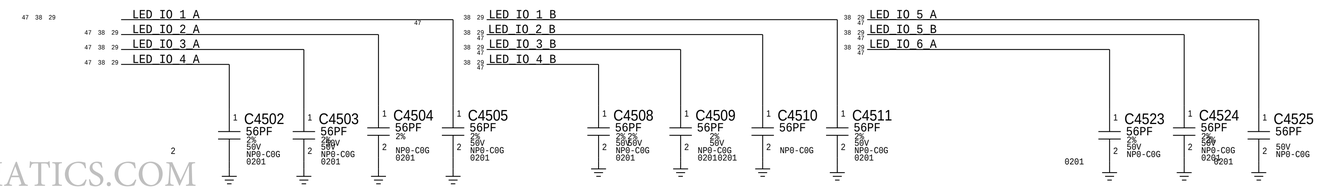
TCON I2C FILTERS





DISPLAY ID
---
0 - X1452 (OXIDE DISPLAY)
1 - X1449 (A-SI DISPLAY)

LED DRIVER FILTERS



SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018

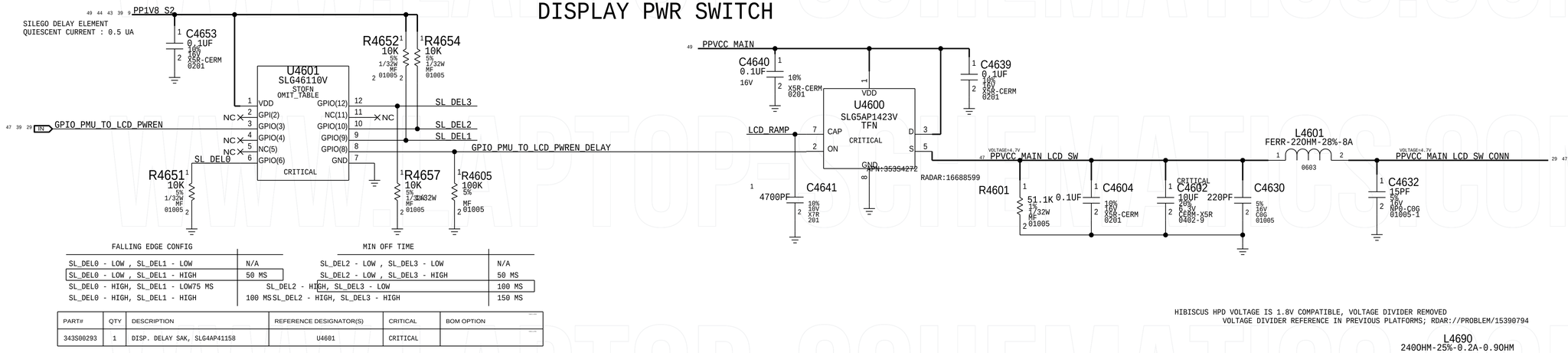
PAGE TITLE

DISPLAY CONN

EDP CONNECTOR SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897		L4602,ETC	RADAR://PROBLEM/21527410

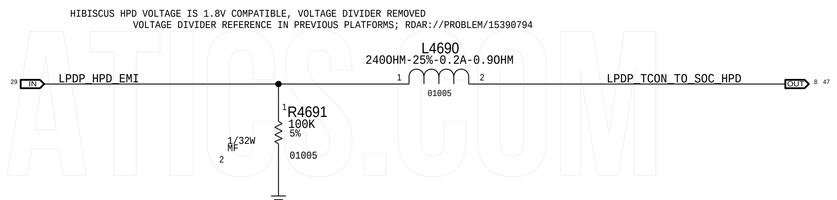
DISPLAY PWR SWITCH



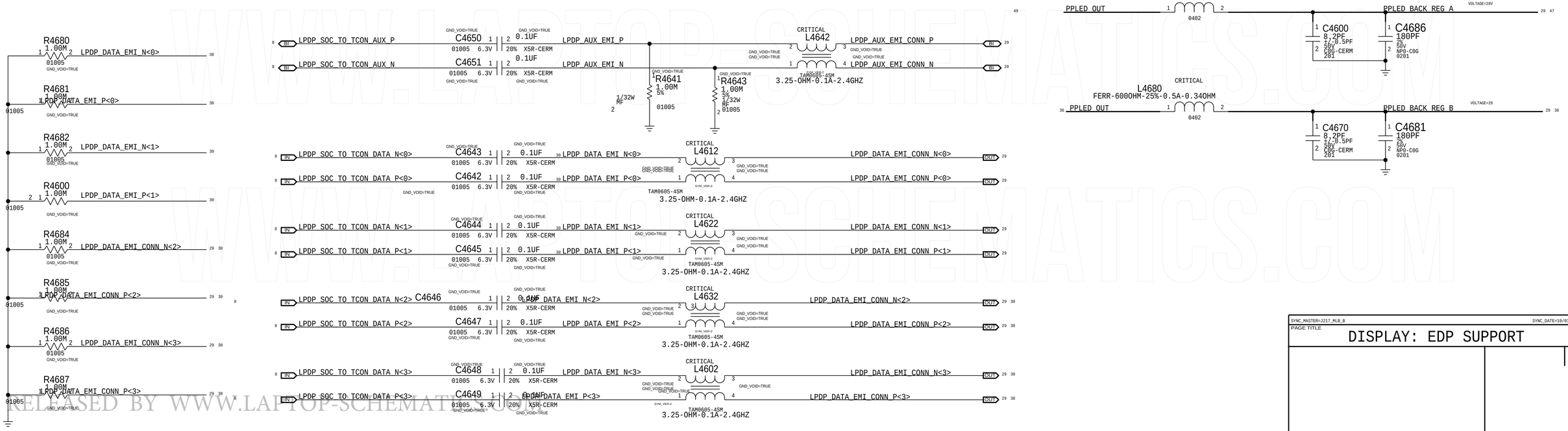
FALLING EDGE CONFIG		MIN OFF TIME	
SL_DEL0 - LOW , SL_DEL1 - LOW	N/A	SL_DEL2 - LOW , SL_DEL3 - LOW	N/A
SL_DEL0 - LOW , SL_DEL1 - HIGH	50 MS	SL_DEL2 - LOW , SL_DEL3 - HIGH	50 MS
SL_DEL0 - HIGH, SL_DEL1 - LOW75 MS		SL_DEL2 - HIGH, SL_DEL3 - LOW	100 MS
SL_DEL0 - HIGH, SL_DEL1 - HIGH	100 MS	SL_DEL2 - HIGH, SL_DEL3 - HIGH	150 MS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00293	1	DISP. DELAY SAK, SLG4AP41158	U4601	CRITICAL	

HIBISCUS HPD VOLTAGE IS 1.8V COMPATIBLE, VOLTAGE DIVIDER REMOVED
VOLTAGE DIVIDER REFERENCE IN PREVIOUS PLATFORMS; RDAR://PROBLEM/15390794



LPDP-AC COUPLING & CMC



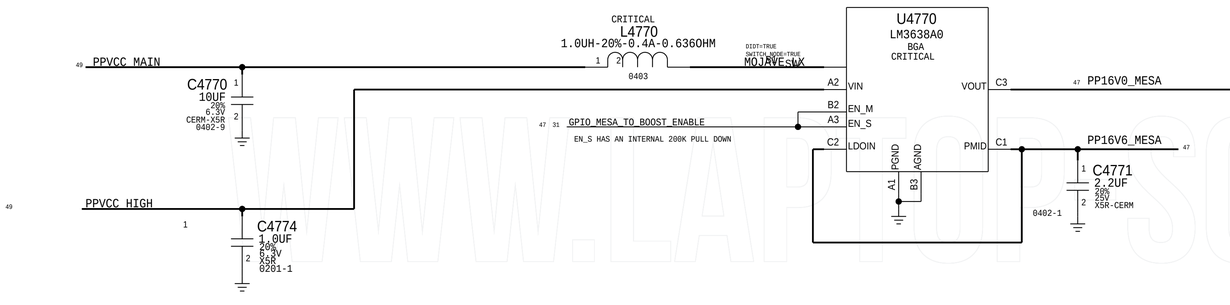
SYNC_MASTER=J217_MLB_B	SYNC_DATE=10/01/2018
PAGE TITLE	DISPLAY: EDP SUPPORT

MESA & HOME BUTTON

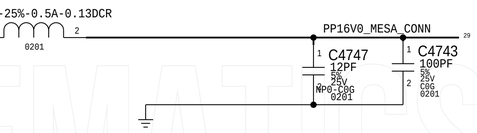
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00088	132S0639		C4746, ETC	RDAR://PROBLEM/26928883

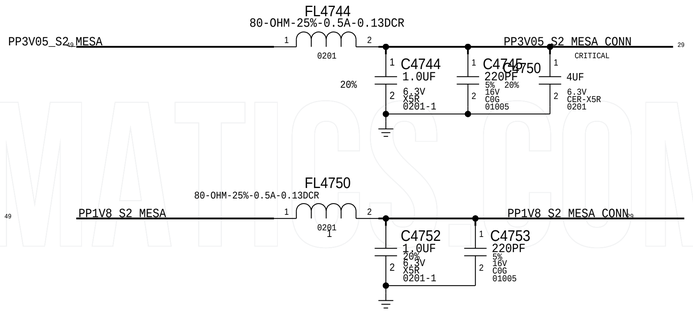
MOJAVE

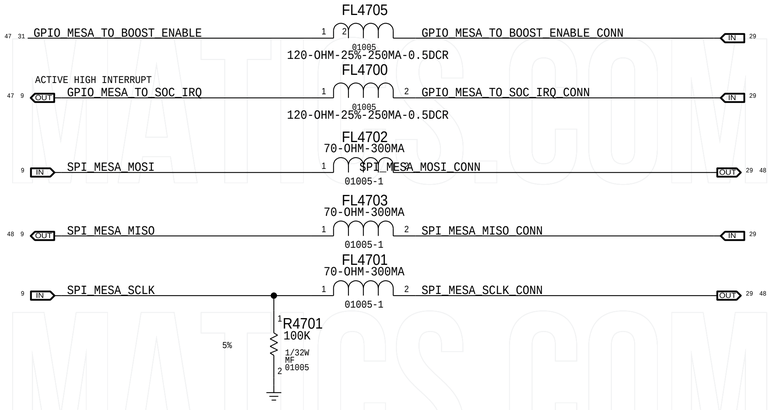
USING A0 (APN 353S00671)



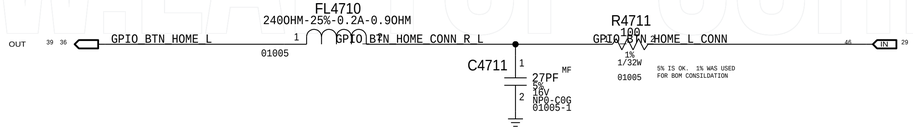
FILTERS







HOME BUTTON FILTERS



SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

SENSOR: MESA

WLAN SYMBOL IO PORTS

POWER

50 45 34 33 IO PPVCC_MAIN
VOLTAGE=3.8

45 IO PP1V8_S3_EXT_SW2
VOLTAGE=1.8

CONTROL

45 33 IO GPIO_PMU_TO_WLAN_REG_ON
45 33 IO GPIO_PMU_TO_BT_REG_ON
45 33 IO GPIO_SOC_BT_DEVICE_WAKE

CLOCKS

45 33 IO CLK_PMU_TO_WLAN_32K
GPIO_WLAN_TO_SOC_TIME_SYNC
45 33 IO

WLAN PCIE

45 33 IO PCIE_SOC_TO_WLAN_REFCLK_P
45 33 IO PCIE_SOC_TO_WLAN_REFCLK_N
45 33 IO PCIE_SOC_TO_WLAN_TX_P
45 33 IO PCIE_SOC_TO_WLAN_TX_N
45 33 IO PCIE_WLAN_TO_SOC_TX_C_P
45 33 IO PCIE_WLAN_TO_SOC_TX_C_N
IO 45 33 PCIE_SOC_TO_WLAN_RESET_L
IO 45 33 PCIE_WLAN_TO_SOC_CLKREQ_L
IO 45 33 GPIO_WLAN_TO_PMU_HOST_WAKE

BLWLAN UART

45 33 IO UART_SOC_TO_BT_TX
45 33 IO UART_BT_TO_SOC_TX
45 33 IO UART_SOC_TO_BT_RTS_L
45 33 IO UART_BT_TO_SOC_RTS_L

AOP

IO 45 33 GPIO_AOP_TO_WLAN_CONTEXT_A
IO 45 33 GPIO_AOP_TO_WLAN_CONTEXT_B

COEX

46 33 IO NC_UART_COEX_BB_TO_WLAN_TXD
46 33 IO NC_UART_COEX_WLAN_TO_BB_TXD

RF

IO 50 PRX_LAA_LNA2_OUT
IO 50 PRX_LAA_LNA1_OUT

RFFE

IO LAT_LAA_RFFE_VIO
34 32 IO UAT_LAA_RFFE_CLK
34 32 IO UAT_LAA_RFFE_DATA
34 IO UAT_LAA_RFFE_VIO
34 32 IO UAT_LAA_RFFE_CLK
34 32 IO UAT_LAA_RFFE_DATA

PENCIL

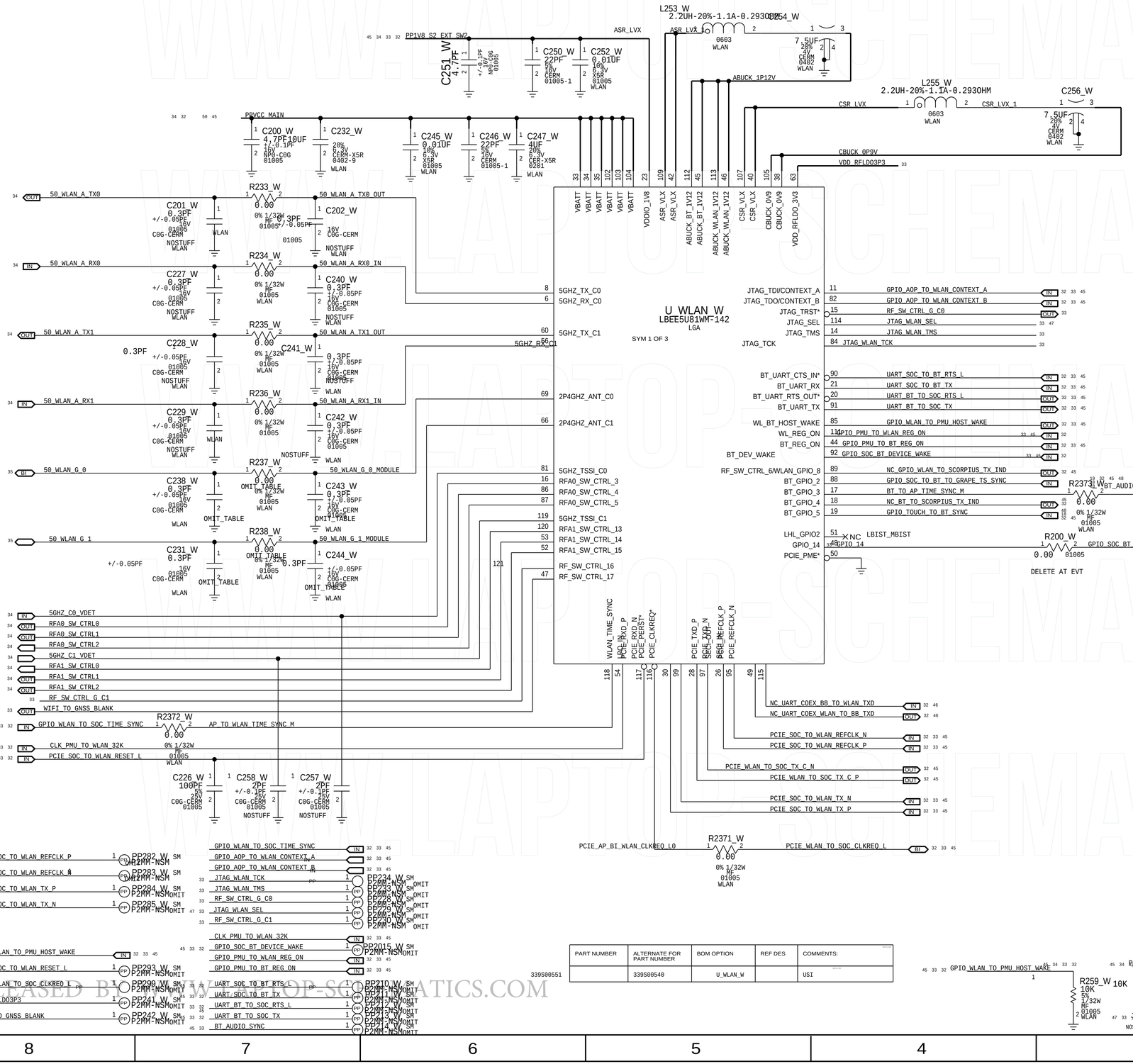
10 45 33 19 18 48 IO GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC
48 45 33 18 IO GPIO_TOUCH_TO_BT_SYNC
45 33 IO NC_BT_TO_SCORPIUS_TX_IND
45 33 IO NC_GPIO_WLAN_TO_SCORPIUS_TX_IND

SYNC_MASTER=WIFI_MLB_0.22.0 SYNC_DATE=09/26/2018

PAGE TITLE

J217+J218 WiFi+BT_GNSS

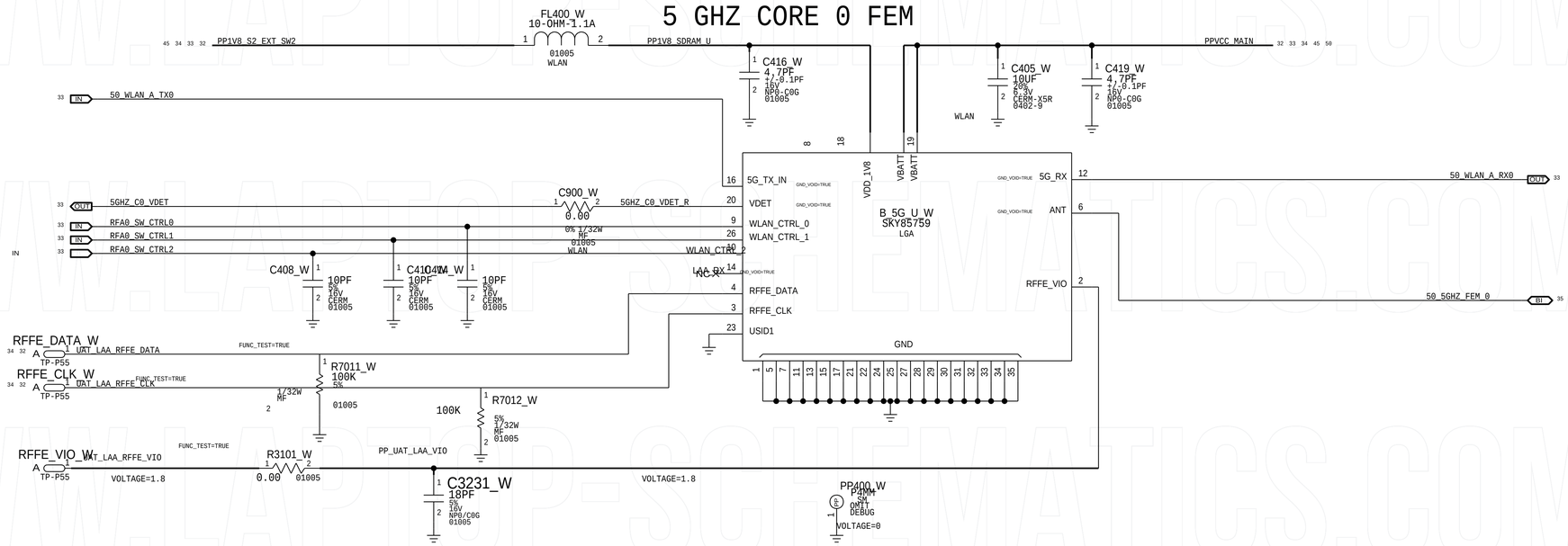
J217+J218: DIET COKE PRIMARY MODULE



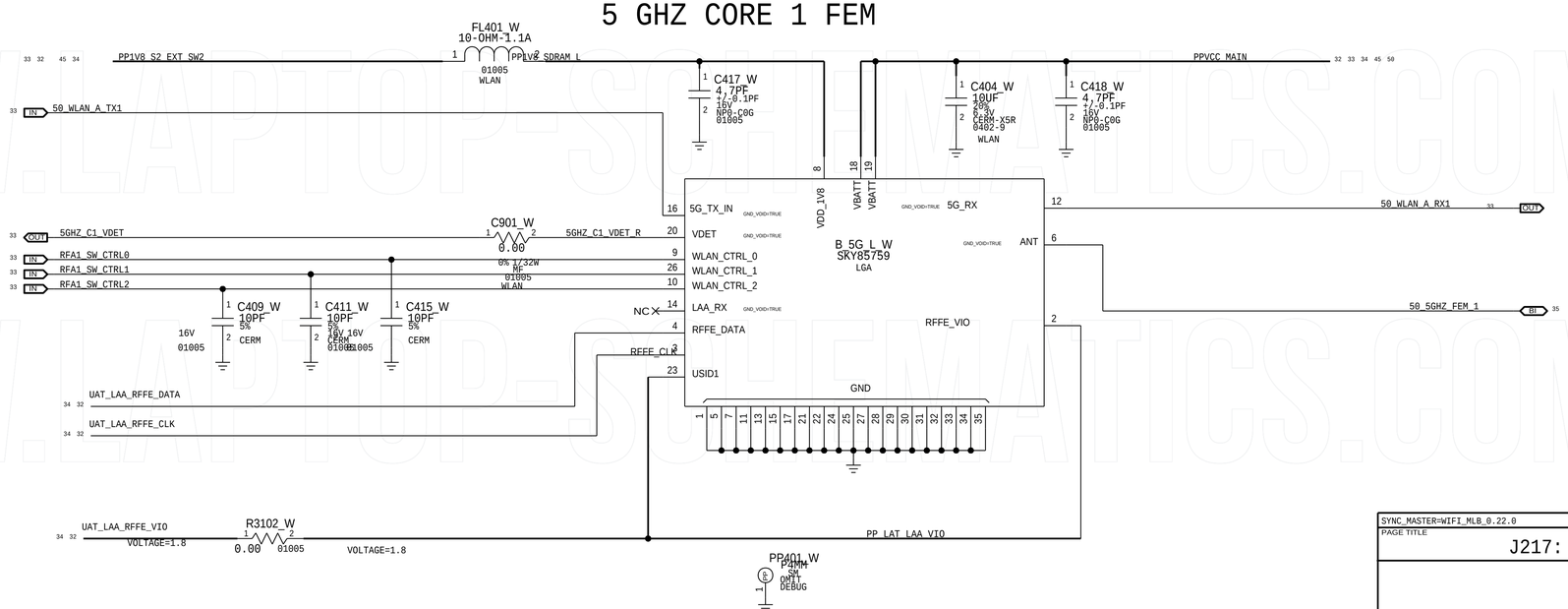
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
	339S00540	U_WLAN_W		USI

J218: DIET COKE REMOTE FEMS

5 GHZ CORE 0 FEM



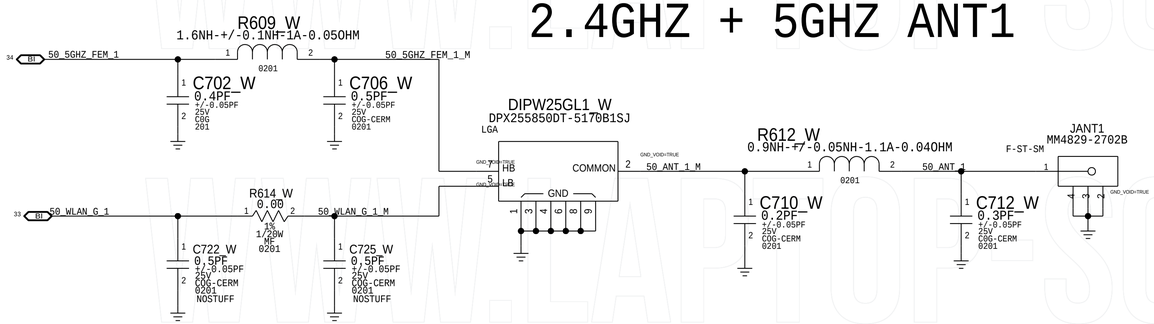
5 GHZ CORE 1 FEM



SYNC_MASTER=WIFI_MLB_0.22.0	SYNC_DATE=09/26/2018
PAGE TITLE	
J217: Remote FEMs	

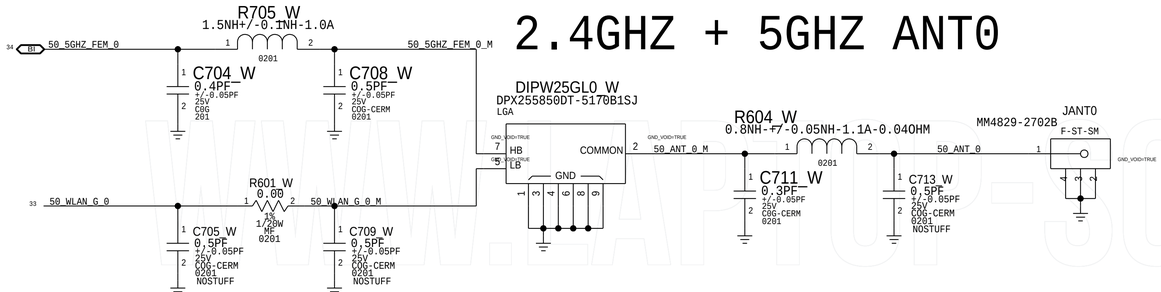
J217: FRONT END

2.4GHZ + 5GHZ ANT1



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00030	1	NOSTUFF	C243_W	NOSTUFF
131S0893	1	CAP,CER,C0G,0.2PF,01005,HQ	C238_W	
152S00427	1	IND,FILM,2.0NH,+/-0.1NH,SHQ,01005	R237_W	
152S00431	1	IND,FILM,2.4NH,+/-0.1NH,,01005	R238_W	
131S0893	1	CAP,CER,C0G,0.2PF,,01005,HQ	C244_W	
131S0893	1	CAP,CER,C0G,0.2PF,01005,HQ	C231_W	

2.4GHZ + 5GHZ ANT0



SYNC_MASTER=WIFI_MLB_0.22.0	SYNC_DATE=09/26/2018
PAGE TITLE	J217: Front End

BUCK3 (SLEEP2)

PP1V8_S2 — PP1V8_S2 (MAKE_BASE=TRUE)

BACKLIGHT BOOST

PPLED_OUT — PPLED_OUT (MAKE_BASE=TRUE)

CHARGER MAIN

PPVCC_MAIN — PPVCC_MAIN (MAKE_BASE=TRUE)

GPIO_BRD_ID3 — GPIO_BRD_ID3 (MAKE_BASE=TRUE)

GPIO_ALS_C4_TO_SOC_IRQ_L (IN) — GPIO_ALS_C4_TO_SOC_IRQ_L (OUT)

GPIO_ALS_C3_TO_SOC_IRQ_L (IN) — GPIO_ALS_C3_TO_SOC_IRQ_L (OUT)

TP93I7 CLK_SOC_TO_REAR_CAM_12MHZ
TP93I8 ISP_I2C0_SCL_1V8
TP93I9 ISP_I2C0_SDA_1V8
TP93J0 GPIO_SOC_TO_REAR_CAM_SHTDWN_L

TP93G4 GPIO_BTN_HOME_L
TP93G5 GPIO_BTN_ONOFF_L
TP93G6 GPIO_BTN_VOL_UP_L
TP93G7 GPIO_BTN_VOL_DOWN_L

PP1V8_EXT_SW1 — R1000 2.2K 5% 1/32W MF 01005 — R1001 2.2K 5% MF 01005

I2C0_SCL_1V8
I2C0_SDA_1V8

TP93X0 CCG2_TO_HYDRA_CC

L3590 FERR-220HM-28%-8A 0603
PPVBUS_USB_EMI — PPVBUS_E75_USB_CONN

L82R0 4.7UH-20%-2.5A-0.12OHM PIHA041B-1 (APN: 152S00957)
PPVCC_MAIN — WLED_LX_B (DIDT=TRUE, SWITCH_NODE=TRUE)
C82R6 10UF 20% 6.3V CERM-X5R 0402-9
C82S2 330PF 10% 16V CER-X7R 01005
R82S3 10 5% 1/32W MF 01005 (NOSTUFF)
D82R0 PMEG4010BEA/S501 SOD323 (RC82S3)
C82S3 100PF 5% 50V C0G 0201

PPLED_OUT
C82R0 10UF 20% 35V XSR-CERM 0603
C82R1 10UF 20% 35V XSR-CERM 0603
C82R2 10UF 20% 35V XSR-CERM 0603
C82R3 10UF 20% 35V XSR-CERM 0603
C82R4 10UF 20% 35V NPO-C0G 0603
C82R5 180PF 2% 50V C0G 0201

PP1V1_S2
C14Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C14Z1 15PF 5% 50V C0G 0201
C14Z2 100PF 5% 50V C0G 0201

PPVDD_S1_FIXED
C14Z5 2.7PF +/-0.1PF 25V C0G-CERM 0201
C14Z6 15PF 5% 50V C0G 0201
C14Z7 100PF 5% 50V C0G 0201

PPVDD_S1_FIXED
C07Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C07Z1 15PF 5% 50V C0G 0201
C07Z2 100PF 5% 50V C0G 0201

PPVDD_S1_SOC
C13Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C13Z1 100PF 5% 50V C0G 0201

PPVDD_S1_FIXED
C08Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C08Z1 15PF 5% 50V C0G 0201
C08Z2 100PF 5% 50V C0G 0201

PP1V8_S2
C12Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C12Z1 15PF 5% 50V C0G 0201
C12Z2 100PF 5% 50V C0G 0201

PPVDD_S1_FIXED
C09Z0 2.7PF +/-0.1PF 25V C0G-CERM 0201
C09Z1 15PF 5% 50V C0G 0201
C09Z2 100PF 5% 50V C0G 0201

PPVCC_MAIN — C8070 1UF 20% 10V X5R 0201
PP1V8_INT_ORION — C8071 1.0UF 20% 6.3V X5R 0201-1

PP1V8_S2 — C8072 1UF 20% 6.3V X5R 0201

PPVBUS_PROT — C8023 0.1UF 10% 25V X5R 0201

PPVBUS_PROT — XW8000 (NO_XNET_CONNECTION=1) SM — PPVDD_USBPD_DET (VOLTAGE=15)

Q8001 CRITICAL CSD58900L LGA — PPVBUS_USB_RVP
EXT_PWRIN_EN1
EXT_PWRIN_EN2

Q8061 CRITICAL POWERDI3333 DMP3013SFV-X-55 — PPVBUS_USB_EMI
DZ8061 CRITICAL BZT52C10LP DFN1006Z
E75_RVP_G
R8061 220K 1% 1/20W MF 201 — FOR CONTAMINATION RESISTANCE MEASUREMENT

Q8000 CRITICAL CSD58900L LGA — PPVBUS_ORION_RVP
ACC_PWRIN_EN1
ACC_PWRIN_EN2

Q8051 CRITICAL CSD68832L LGA — PPVBUS_ORION (VOLTAGE=14.5)
DZ8051 CRITICAL BZT52C10LP DFN1006Z — NOTE: 10V ZENER
R8060 499 1% 1/10W MF-LF 603
R8051 220K 1% 1/20W MF 201

PPVBUS_USB_RVP_R (VOLTAGE=15) — R8020 0.00 0% 1/32W MF 01005 — PPVBUS_USB_RVP (FROM E75 RVP FET)
C8020 1.0UF 20% 35V CERM-X5R 0402

PPVCC_MAIN — C8070 1UF 20% 10V X5R 0201
PP1V8_INT_ORION — C8071 1.0UF 20% 6.3V X5R 0201-1

BELLATRIX

U8000 CRITICAL CD3257 WCSP

VP			
(VDD_INT_CWB)			
VDD_IO			
HWEN (TO BE SET TO HIGH BY DEF) 2M INT PD			
INT	GPIO_ORION_TO_AOP_IRQ		
SCL	I2C2_SCL_1V8		
SDA	I2C2_SDA_1V8	GND/DFT	
VBUS_VALID*		(INTERNAL PD)	ACC_PWR_EN_L
EXT_VBUS_VALID* (100K INT PD)			
CONN_STATUS*(OUTPUT)	TP_ORION_CONN_STATUS		ACC_PWR_PRESENT_L/ADC_CH1 (OD OUTPUT)
HS_RX_OUT (I/O - HI-Z GPOR)	UART_BELLATRIX2_TO_SOC_TX		
HS_TX_IN	UART_SOC_TO_BELLATRIX2_TX		
DATA			ORION_COMM_FILT

R8070 100K 5% 1/32W MF 01005 — GPIO_AOP_TO_ORION_HWEN
R8071 2.0K 1% 1/32W MF 01005 — HYDRA_OVP_SW_EN_L
R807A 1.00K 5% 1/32W MF 01005 — GPIO_PMU_TO_ORION_VBUS_VALID_L
D8000 CRITICAL SOD962-2 PMEG3002ESF

R8022 100K 5% 1/32W MF 01005 (NOSTUFF) — GPIO_PMU_TO_ORION_ACC_PWR_EN_L
GPIO_ORION_TO_PMU_ACC_PWR_PRES_L

ORION_RVP
ORION_RVP_G

POWER - CAMERA (ARIZONA) - DIFF NAMES FROM J211
TP9353 PP1V25_REAR_CAM
REMOVED TP9357-PP2V9_REAR_CAM_CONN
REMOVED TP9355-PP2V6_REAR_CAM_AP_CONN
REMOVED TP9354-PP1V8_REAR_CONN

ORION
TP939F TP-1P0-TOP
TP939C TP-1P0-TOP — PPVBUS_ORION_CONN
TP939G TP-1P0-TOP

J217-SPECIFIC PPS

ORION
PP9500 P3MM SM
PP953B P4MM SM — GPIO_AOP_TO_ORION_HWEN

KONA SLAVE
PP958U KONA_S_VDDCORE_CAP
PP9586 KONA_S_TO_KONA_M_RESET_DET_L
PP9587 PSE_SYNC
PP9588 KMSI_MISO
PP9589 KMSI_MOSI
PP958A KMSI_STRB_IN
PP958B KMSI_STRB_OUT
PP958D TP_KONA_S_UART_TX
PP958E TP_KONA_S_UART_RX
PP958F TP_KONA_IPC_EVENT_0
PP958G TP_KONA_IPC_EVENT_1
PP958H TP_KONA_IPC_EVENT_2
PP958I TP_KONA_IPC_EVENT_3
PP958J TP_KONA_IPC_EVENT_4
PP958K TP_KONA_IPC_EVENT_5

PP0V9_NAND — C1708 4.7PF +/-0.1PF 10V NP0-C0G 01005 ROOM=NAND
PP1V8_EXT_SW1 — C1715 4.7PF +/-0.1PF 16V NP0-C0G 01005 ROOM=NAND
PP2V63_NAND — C1734 4.7PF +/-0.1PF 16V NP0-C0G 01005 ROOM=NAND

J217-SPECIFIC TPS

TP93N3 PP2V8_KONA_S_VDDANA
TP93J5 GPIO_CPANEL_HALL_TO_PMU_IRQ_L
TP93J6 GPIO_APANEL_HALL_TO_PMU_IRQ_L
TP93EG PPVBUS_ORION_RVP
TP93EH PPVBUS_ORION_CONN
TP93E4 ORION_COMM_CONN
TP93EA GPIO_ORION_TO_AOP_IRQ
TP93EF PP1V8_INT_ORION
TP93G3 PP1V8_S2_MIC_MOLYBDENUM
TP93G8 I2C0_SCL_1V8
TP93G9 I2C0_SDA_1V8
TP936A PPLED_BACK_REG_B
TP936B PPLED_BACK_REG_B

ATLAS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00281	1	IC,PMU,ATLAS,D2652A0,OTP-AC,CSP400	U8100	CRITICAL	

POTOMAC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
1343S00264		IC,POTOMAC,D2559A0,OTP-CC	U8500	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C8070,ECT	

TP93Z0 PPBATT_VCC
TP93Z1
TP93Z2
TP93Z3
TP93Z4
TP93Z6
TP93Z7
TP93Z5

TP93Z8 BATT_SDA_CONN
TP93Z9 BATT_SCL_CONN
TP93ZA PP1V8_GRAPE
TP93ZB PP3V3_GRAPE

C3545 100PF 5% 50V C0G 0201 — PPVBUS_E75_USB_CONN

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
ORION & J217-J218 UNIQUE

ATLAS BUCKS

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: ATLAS (1/3)

ATLAS LDOS (2/3)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0703	138S0648		C8233,ECT	ALT FOR 4.7UF,6.3V,0402

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: ATLAS (2/3)

ATLAS (3/3)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: ATLAS (3/3)

POTOMAC/RENO

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00071	376S00070		Q8581,ECT	RDAR://PROBLEM/20277540

U8500
D2559A0P0V2AVAC2
WLCSP
OMIT_TABLE

PPVBUS_PROT
C8500 10UF 20% 35V X5R-CERM 0603 CRITICAL
C8501 10UF 20% 35V X5R-CERM 0603 CRITICAL
C8502 10UF 20% 35V X5R-CERM 0603 CRITICAL

R8520 0.00 0% 1/32W 01005 MF
ORION_TO_POTOMAC_OVP_SW_EN_L
ORION_TO_POTOMAC_OVP_SW_EN_L_R
R8521 0.00 0% 1/32W 01005 MF
GPIO_PMU_TO_POTOMAC_LINCH_EN
GPIO_PMU_TO_POTOMAC_LINCH_EN_R
R8523 0.00 0% 1/32W 01005 MF
PP1V8_SW1
NC_GPIO_POTOMAC_TO_PMU_VSYS_HI_SW
GPIO_PMU_TO_POTOMAC_BOOST_EN
GPIO_POTOMAC_TO_SMC_TO_PMU_IRQ_L
I2C_SMC_I2CM0_SCL_1V8
I2C_SMC_I2CM0_SDA_1V8
BATT_NTC_POS
PPVDD_REF_CHG
PPVDD_POTOMAC_GPIO
PPVDD_POTOMAC_CORE
POTOMAC_IREF
POTOMAC_VREF
POTOMAC_ADC_REF
NC_POTOMAC_BOOST_PRE_UVLO
ATLAS_TO_POTOMAC_CRASH_L
GPIO_POTOMAC_TO_PMU_WAKE
USB_VBUS_DETECT
GPIO_POTOMAC_TO_SMC_TO_PMU_IRQ_L

VBUS_OVP_OFF(GPIO1)
CRASH(GPIO2)
VSYS_HI_UVLO(GPIO3)
LINCH_EN(GPIO4)
WAKEUP(GPIO5)
USB_VBUS_DET(GPIO6)
HV_CHG_OVERRIDE(GPIO7)
BOOST_EN(GPIO8)
IRQ*
SCL
SDA
TBAT
VDD_REF_CHARGE
VDD_REF_CHARGE_PH0
VDD_REF_CHARGE_PH1
VDD_GPIO
VDDCORE_DIG
IREF
VREF
ADC_REF
ADC_IN_P
ADC_IN_N
H_TEST_MODE
VSSA_2
VSSA_3
VSS_PH0
VSS_PH1
VSS_BUBO
VSS_BOOST
VSS_BG_SENS
VSSD_FRAME
VSS_ESD

C8512 0.1UF 10% 16V X5R-CERM 0201-8
C8513 10UF X5R CRITICAL
C8516 0.1UF 10% 16V X5R-CERM 0201
C8510 0.1UF 10% 16V X5R-CERM 0201
C8511 0.1UF 10% 16V X5R-CERM 0201
R8515 200K 0.5% 1/20W MF 0201
C8515 0.1UF 10% 16V X5R-CERM 0201
C8514 0.1UF 10% 16V X5R-CERM 0201

PP1V8_ALWAYS
R8525 10K 5% 1/32W MF 01005
R8526 10K 5% 1/32W MF 01005

VCENTER_3 VCENTER_0 VCENTER_1
C8555 0.1UF 10% 35V CER-X5R 0201 CRITICAL
C8550 10UF 20% 35V X5R-CERM 0603 CRITICAL
C8557 0.1UF 10% 35V CER-X5R 0201 CRITICAL
C8551 10UF 20% 35V X5R-CERM 0603 CRITICAL
C8556 0.1UF 10% 35V CER-X5R 0201 CRITICAL
C8552 10UF 20% 35V X5R-CERM 0603 CRITICAL
PPVCENTER

VCENTER_1_HS
PPVCENTER_1_HS
C8558 0.1UF 10% 25V X5R CRITICAL

VBOOT_N0 VBOOT_DRV0 LX_BOOT_PH0
POTOMAC_VBOOT0
C8560 0.1UF X5R-CERM 16V 10% 0201 CRITICAL
POTOMAC_VBOOT_PH0

VBOOT_N1 VBOOT_DRV1 LX_BOOT_PH1
POTOMAC_VBOOT1
C8561 0.1UF X5R-CERM 16V 10% 0201 CRITICAL
POTOMAC_VBOOT_PH1

BOOST_HS_SUPPLY
POTOMAC_HS_SUPPLY
BOOST_HS_SOURCE
POTOMAC_HS_SRC
C8562 0.1UF 10% 16V X5R-CERM 0201 CRITICAL

VSYS_HI_S
POTOMAC_VSYS_HI_S
XW8501 SHORT-18L-0.1MM-SM OMIT

VSYS_HI
VSYS_HI_EXT_DIO
POTOMAC_HIGH_DIO
NOSTUFF R8581 470K 5% 1/32W MF 01005
Q8581 FDMC6688P MLP3.3X3.3 CRITICAL

VSYS_LO_BYPASS
L8570 1UH-20%-6.4A-0.038OHM PIKA32251B-SM CRITICAL
POTOMAC_LX_PH0
LX_PH0
POTOMAC_LX_BUBO
LX_BUBO
VSYS_LO_BUBO
C85A3 4.7UF 20% 16V X5R 0402-1 CRITICAL
C8590 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8599 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
LX_BOOST
C859A 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C859B 20UF 20% 6.3V CERM-X5R CRITICAL
C859C 20UF 20% 6.3V CERM-X5R 0402 CRITICAL

L8571 0.47UH-20%-8.6A-0.024OHM PIKA32251B-SM CRITICAL
POTOMAC_LX_PH1
LX_PH1

VSYS_LO_S
POTOMAC_VSYS_LO_S
XW8500 SHORT-18L-0.1MM-SM OMIT

VSYS_LO_EXT_DIO
POTOMAC_LOW_DIO

IBAT_1 IBAT_2
R8593 499 1% 1/20W MF 201
R8592 0.00 0% 1/32W 01005 MF
BATT_SNS_R
BATT_SNS

PPVCC_HIGH
C8567 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8568 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8569 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8563 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8564 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8565 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8566 47UF 20% 6.3V CER-X5R 0603 CRITICAL

C8580 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8588 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8589 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8581 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8582 20UF 20% 6.3V CERM-X5R 0402 CRITICAL
C8583 20UF 20% 6.3V CERM-X5R 0201-1 CRITICAL
C8584 1.0UF 20% 6.3V X5R CRITICAL

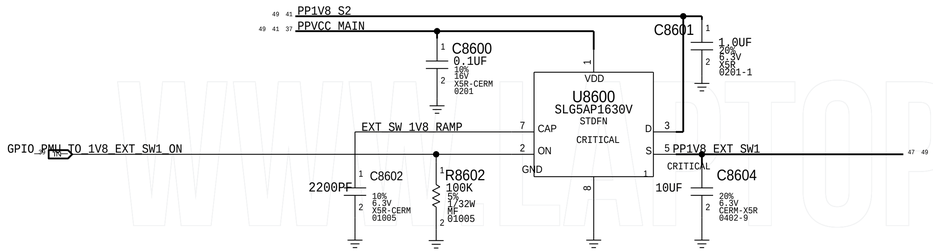
PPVCC_MAIN
C85A0 10UF 20% 10V X5R-CERM 0402-7 CRITICAL
C8570 10UF 20% 10V X5R-CERM 0402-7 CRITICAL
C8571 10UF 20% 10V X5R-CERM CRITICAL
C8572 10UF 20% 10V X5R-CERM 0402-7 CRITICAL
C8573 10UF 20% 10V X5R-CERM CRITICAL
C8574 10UF 20% 10V X5R-CERM 0402-7 CRITICAL
C85A1 10UF 20% 10V X5R-CERM CRITICAL
C85A2 10UF 20% 10V X5R-CERM 0402-7 CRITICAL

NOSTUFF R8580 470K 5% 1/32W MF 01005
Q8580 FDMC6686P POWER33 CRITICAL

PPBATT_VCC
C8593 47UF 20% 6.3V CER-X5R 0603 CRITICAL
C8591 10UF 20% 6.3V CERM-X5R 0402-9 CRITICAL
C8592 10UF 20% 6.3V CERM-X5R 0402-9 CRITICAL
PPBATT_POS_RC
R8591 0.5 1% 1/16W MF 402
NOTE: FOR NO BATTERY SITUATION

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
POWER: CHARGER

EXTERNAL POWER SWITCHES

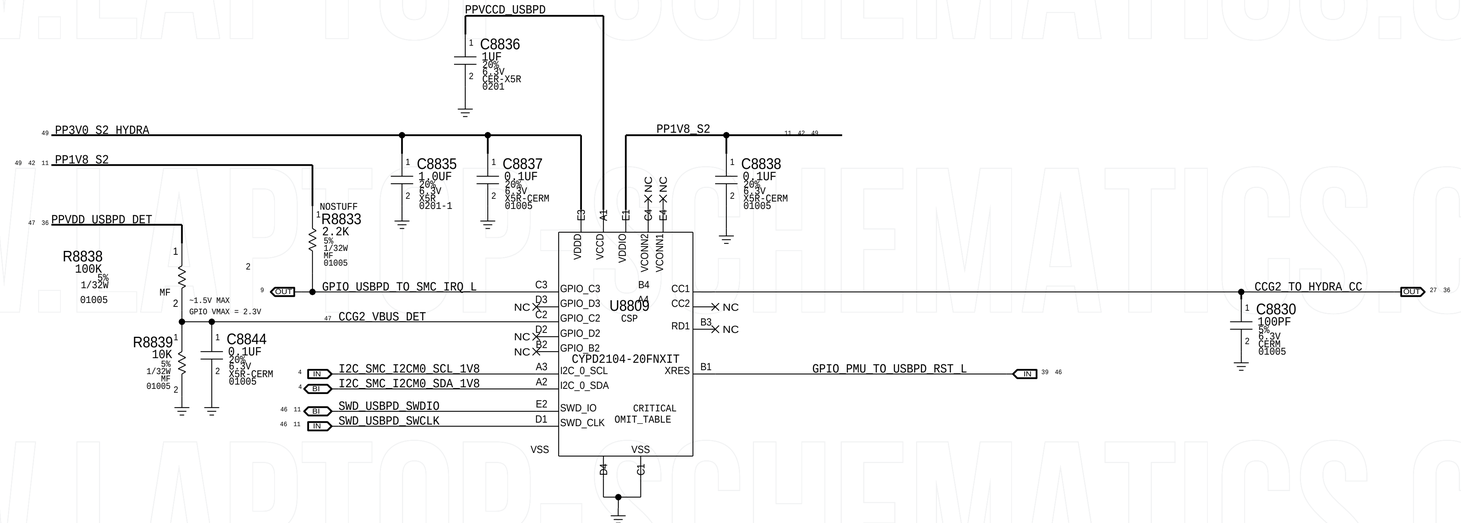


SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: EXTERNAL SWITCHES

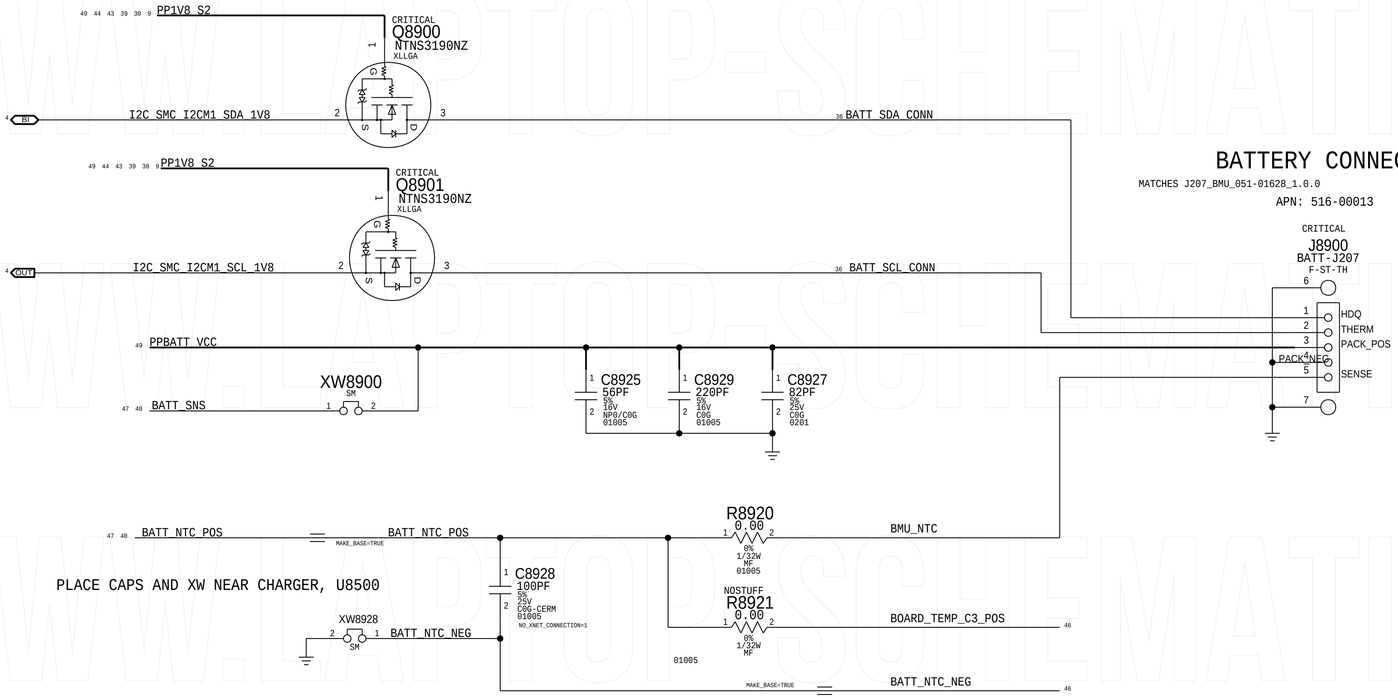
USBPD

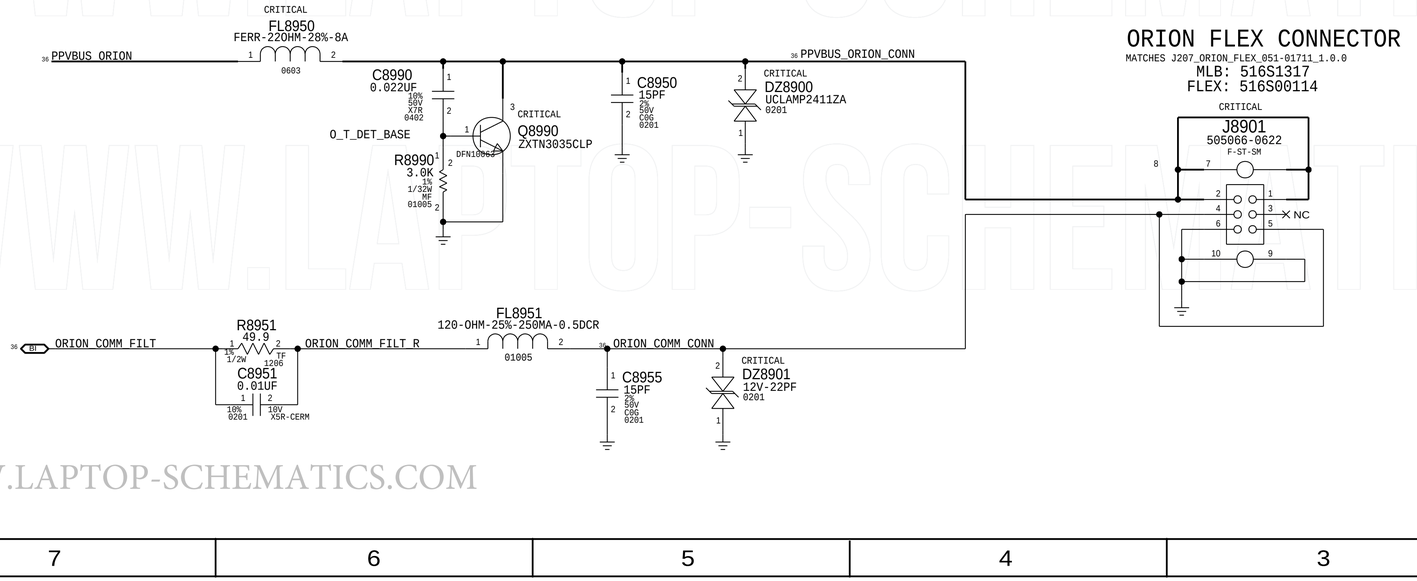


SYNC_MASTER=2217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: USB PD



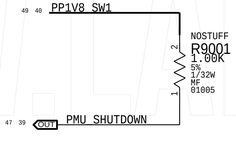


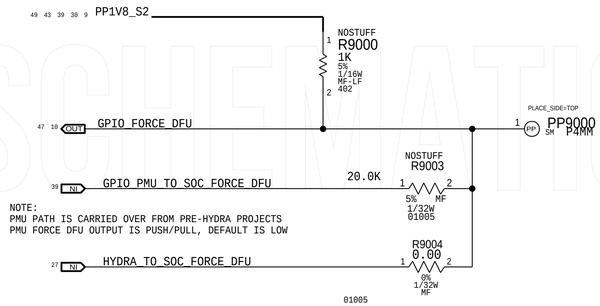
SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

POWER: BATTERY & ORION CONN

DEBUG RESET ACCESS





SYNC_MASTER=2017_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

SOC: DEBUG

WLAN/BT ALIASES

WLAN

POWER

49	PPVCC_MAIN			PPVCC_MAIN	32 33 34 50
49	PP1V8_S2_EXT_SW2			PP1V8_S2_EXT_SW2	32 33 34

GPIOS

47 39	IN	GPIO_PMU_TO_WLAN_REG_ON	MAKE_BASE=TRUE	GPIO_PMU_TO_WLAN_REG_ON	OUT	32 33
47 39	OUT	GPIO_WLAN_TO_PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_WLAN_TO_PMU_HOST_WAKE	IN	32 33
38	IN	CLK_PMU_TO_WLAN_32K	MAKE_BASE=TRUE	CLK_PMU_TO_WLAN_32K	OUT	32 33
47 11	IN	GPIO_AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE	GPIO_AOP_TO_WLAN_CONTEXT_A	OUT	32 33
47 11	IN	GPIO_AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE	GPIO_AOP_TO_WLAN_CONTEXT_B	OUT	32 33
47 10	OUT	GPIO_WLAN_TO_SOC_TIME_SYNC	MAKE_BASE=TRUE	GPIO_WLAN_TO_SOC_TIME_SYNC	IN	32 33
		NC_GPIO_WLAN_TO_SCORPIUS_TX_IND	MAKE_BASE=TRUE	NC_GPIO_WLAN_TO_SCORPIUS_TX_IND	IN	32 33

UART (SHARED WITH BT)

PCIE

6	IN	PCIE_SOC_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_REFCLK_P	OUT	32 33
6	IN	PCIE_SOC_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_REFCLK_N	OUT	32 33
6	IN	PCIE_SOC_TO_WLAN_TX_P	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_TX_P	OUT	32 33
6	IN	PCIE_SOC_TO_WLAN_TX_N	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_TX_N	OUT	32 33
45	IN	PCIE_WLAN_TO_SOC_TX_C_P	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_TX_C_P	IN	32 33
45	IN	PCIE_WLAN_TO_SOC_TX_C_N	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_TX_C_N	IN	32 33
48 6	OUT	PCIE_WLAN_TO_SOC_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN_TO_SOC_CLKREQ_L	IN	32 33
48 6	IN	PCIE_SOC_TO_WLAN_RESET_L	MAKE_BASE=TRUE	PCIE_SOC_TO_WLAN_RESET_L	OUT	32 33

GND_VOID=TRUE

48 6 PCIE_WLAN_TO_SOC_TX_P — C9160 1 2 0.1UF — PCIE_WLAN_TO_SOC_TX_C_P 45
6.3V 20% X5R-CERM 01005

48 6 PCIE_WLAN_TO_SOC_TX_N — C9161 1 2 0.1UF — PCIE_WLAN_TO_SOC_TX_C_N 45
20% 6.3V X5R-CERM 01005 GND_VOID=TRUE

BLUETOOTH

SOC GPIOS

DIETCOKE COMBINES BT AND WLAN WAKE TO PMU

47 39	IN	GPIO_PMU_TO_BT_REG_ON	MAKE_BASE=TRUE	GPIO_PMU_TO_BT_REG_ON	OUT	32 33
10	IN	GPIO_SOC_BT_DEVICE_WAKE	MAKE_BASE=TRUE	GPIO_SOC_BT_DEVICE_WAKE	OUT	32 33

UART

10	IN	UART_SOC_TO_BT_TX	MAKE_BASE=TRUE	UART_SOC_TO_BT_TX	OUT	32 33
10	IN	UART_SOC_TO_BT_RTS_L	MAKE_BASE=TRUE	UART_SOC_TO_BT_RTS_L	OUT	32 33
10	OUT	UART_BT_TO_SOC_TX	MAKE_BASE=TRUE	UART_BT_TO_SOC_TX	IN	32 33
10	OUT	UART_BT_TO_SOC_RTS_L	MAKE_BASE=TRUE	UART_BT_TO_SOC_RTS_L	IN	32 33
48 45 33 32 19 18 10	IN	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC	MAKE_BASE=TRUE	GPIO_SOC_TO_BT_TO_GRAPE_TS_SYNC	OUT	10 18 19 32 33 45 48
48 45 33 32 18	IN	GPIO_TOUCH_TO_BT_SYNC	MAKE_BASE=TRUE	GPIO_TOUCH_TO_BT_SYNC	OUT	18 32 33 45 48
		NC_BT_TO_SCORPIUS_TX_IND	MAKE_BASE=TRUE	NC_BT_TO_SCORPIUS_TX_IND	IN	32 33
10	OUT	BT_AUDIO_SYNC	MAKE_BASE=TRUE	BT_AUDIO_SYNC	IN	33

ROTTERDAM

POWER

PPVCC_MAIN = PP_VDD_MAIN (VCCMAIN ROTTERDAM CONNECTED THROUGH RADIO PPVCC_MAIN ALIAS)

49	PP1V8_S2_EXT_SW2			PP1V8_S2_EXT_SW2	50

GPIOS

50 45 9	IN	GPIO_SOC_TO_ROTTERDAM_DEV_WAKE	MAKE_BASE=TRUE	GPIO_SOC_TO_ROTTERDAM_DEV_WAKE	OUT	9 45 50
50 45 10	IN	GPIO_SOC_TO_ROTTERDAM_DWLD_REQ	MAKE_BASE=TRUE	GPIO_SOC_TO_ROTTERDAM_DWLD_REQ	OUT	10 45 50
39	IN	GPIO_PMU_TO_ROTTERDAM_EN	MAKE_BASE=TRUE	GPIO_PMU_TO_ROTTERDAM_EN	OUT	50

UART

50 45 10	IN	UART_SOC_TO_ROTTERDAM_TX	MAKE_BASE=TRUE	UART_SOC_TO_ROTTERDAM_TX	OUT	10 45 50
50 45 10	OUT	UART_ROTTERDAM_TO_SOC_TX	MAKE_BASE=TRUE	UART_ROTTERDAM_TO_SOC_TX	IN	10 45 50
50 45 10	IN	UART_SOC_TO_ROTTERDAM_RTS_L	MAKE_BASE=TRUE	UART_SOC_TO_ROTTERDAM_RTS_L	OUT	10 45 50
50 45 10	OUT	UART_ROTTERDAM_TO_SOC_RTS_L	MAKE_BASE=TRUE	UART_ROTTERDAM_TO_SOC_RTS_L	IN	10 45 50

SYNC_MASTER=J217_MLB_B SYNC_DATE=10/01/2018

PAGE TITLE

ALIASES: WLAN/BT

BOARD ID

PP1V8_EXT_SW1

R0514	1.00K	5% 1/32W MF 01005
R0513	1.00K	5% 1/32W MF 01005
R0512	1.00K	5% 1/32W MF 01005
R0511	1.00K	5% 1/32W MF 01005

- GPIO_BRD_ID4
- GPIO_BRD_ID3
- GPIO_BRD_ID2
- GPIO_BRD_ID1
- GPIO_BRD_ID0 = 0

BRD_ID[4-0]	
CURRENT SETTING ---> 11100	J217 AP
11101	J217 DEV
11110	J218 AP
J218 DEV	

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

SOC GPIOS

- GPIO_SOC_TO_BB_SDWN_L
- GPIO_SOC_TO_BB_RESET_L
- NC_BB_TO_AP_RESET_DETECT_L
- GPIO_SOC_TO_BB_COREDUMP
- NC_AP_TO_BB_MESA_ON
- NC_SWD_JTAG_BB_TMS_SWDIO
- NC_APPMU_TO_BBPMU_ON
- NC_PCIE_BB_TO_APPMU_WAKE_L
- NC_UART_AOP_TO_BB_TXD
- NC_UART_BB_TO_AOP_TXD

GPIO_SOC_TO_KONA_DISPLAY_BSYNC1 = AP_TO_BBPMU_FORCE_PWM

POWER

PCIE

- NC_90_PCIE_AP_TO_BB_REFCLK_P
- NC_90_PCIE_AP_TO_BB_REFCLK_N
- NC_PCIE_AP_BI_BB_CLKREQ_L
- NC_PCIE_AP_TO_BB_PERST_L
- NC_90_PCIE_AP_TO_BB_TX_P
- NC_90_PCIE_AP_TO_BB_TX_N
- NC_90_PCIE_BB_TO_AP_TX_P
- NC_90_PCIE_BB_TO_AP_TX_N

PP3V3_USB

C06Z0 12PF 5% 16V NP0-C0G 01005-1

PPVDD_S1_QL

C14Z3 2.7PF +/-0.1PF 25V C0G-CERM 0201

C14Z4 12PF 5% 25V NP0-C0G 0201

PP1V8_EXT_SW1

C06Z1 12PF 5% 16V NP0-C0G 01005-1

PMU ADC

- NC_ADC_BB_TO_PMU_PP_1V85
- NC_ADC_BB_TO_PMU_SW1_VOUT
- NC_ADC_BB_TO_PMU_SW3_VOUT

SIM CARD

TP'S

TP93H0 TP93H1 TP93H2 TP93H3 TP93H6 TP93H7 TP93H8 TP93H9

PP'S

TP'S

- TP93Y5 DUMMY_NET_TP93Y5
- TP93Y6 DUMMY_NET_TP93Y6
- TP93Y7 DUMMY_NET_TP93Y7
- TP93X4 GPIO_BTN_HOME_L_CONN
- TP93X5 GPIO_BTN_ONOFF_L_CONN
- TP93X6 GPIO_BTN_VOL_UP_L_CONN
- TP93X7 GPIO_BTN_VOL_DOWN_L_CONN
- TP93X8 SWD_USBPD_SWDIO
- TP93X9 SWD_USBPD_SWCLK
- TP93XA GPIO_PMU_TO_USBPD_RST_L

RCAM ARIZONA

REAR_CAM_FLEX APN: 516S0750
MLB APN: 516S00073

J2790
AA07A-S026VA1
F-ST-SM1

- CLK_SOC_TO_REAR_CAM_12MHZ_CONN
- GPIO_SOC_TO_REAR_CAM_SHTDWN_L_CONN
- ISP_REAR_CAM_SDA_CONN
- ISP_REAR_CAM_SCL_CONN
- PP1V8_REAR_CAM_CONN
- PP2V6_REAR_CAM_AF_CONN
- PP1V25_REAR_CAM_CONN
- MIPI_CAM_REAR_TO_MINION_DATA_N<3>
- MIPI_CAM_REAR_TO_MINION_DATA_P<3>
- MIPI_CAM_REAR_TO_MINION_DATA_N<0>
- MIPI_CAM_REAR_TO_MINION_DATA_P<0>
- MIPI_CAM_REAR_TO_MINION_DATA_N<1>
- MIPI_CAM_REAR_TO_MINION_DATA_P<1>
- MIPI_CAM_REAR_TO_MINION_CLK_N
- MIPI_CAM_REAR_TO_MINION_CLK_P
- MIPI_CAM_REAR_TO_MINION_DATA_N<2>
- MIPI_CAM_REAR_TO_MINION_DATA_P<2>
- PP2V9_REAR_CAM_CONN

POWER BUTTON + ALS FLEX

ALS_PWR_FLEX APN: 516S00185
MLB APN: 516S00186

J2791
BM28P0.6-6DS/2-0.35V
F-ST-SM

- GPIO_BTN_ONOFF_L_CONN
- I2C_ALS_SDA_C3_CONN
- GPIO_ALS_C3_TO_SOC_IRQ_L
- PP3V0_C3_ALS_CONN
- I2C_ALS_SCL_C3_CONN

GPS

- NC_UART_AP_TO_GNSS_TXD
- NC_UART_GNSS_TO_AP_TXD
- NC_UART_AP_TO_GNSS_RTS_L
- NC_UART_GNSS_TO_AP_RTS_L
- NC_APPMU_TO_GNSS_EN
- GPIO_SOC_TO_BB_GPS_SYNC
- TP_GPIO_AP_TO_GPS_DEV_WAKE
- NC_GNSS_TO_AP_LOW_PWR_IND

SPARE GPIOS

- GPIO_BB_TO_SOC_COEX_SPARE
- GPIO_SOC_TO_BB_COEX_SPARE
- GPIO_SOC_TO_BB_PEAK_PWR_IND_SPARE

COEX UART: BB - WLAN

- NC_UART_COEX_BB_TO_WLAN_TXD
- NC_UART_COEX_WLAN_TO_BB_TXD

NC_PMU_TDEV1

NOSTUFF
COWLING-HOLDER-STAMPED-MLB-J127
C3_CLIP SM

VOL HALL FLEX

VOL_HALL_FLEX APN: 516S00185
MLB APN: 516S00186

J2792
BM28P0.6-6DS/2-0.35V
F-ST-SM

- GPIO_BTN_VOL_UP_L_CONN
- GPIO_BTN_VOL_DOWN_L_CONN
- PP1V8_S2_BASH_HALL
- GPIO_CPANEL_HALL_TO_PMU_IRQ_L

CAN MOUNTING HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM
APN: 998-2691

SL9300 SL9301 SL9303 SL9304 SL9310 SL9311 SL9320 SL9321
TH-NSP
SL-1.1X0.4-1.4X0.7

FIDUCIALS

FID9300 FID9301 FID9302 FID9303 FID9304 FID9305
FID 0P5SM1P0SQ-NSP

STANDOFFS

STD9312 STD9317 STD9318 STD9319 STD9350 STD9320
3.3X1.8R-1.4ID-1.1H-SM
STDOFF-3.8X2.5R-1.1H-TH

NTC: AMBIENT

R2790 0201
BOARD_TEMP_C3_POS — BATT_NTC_NEG
10KOHM-1%-0.31MA

CORNER 4 B2B

MLB APN: 516S00310
FLEX APN: 516S00309
MATCHED TO J217_C4_FLEX_WIFI_1.0.0

CRITICAL
J3150
AA27DK-S024VA1
F-ST-SM

- CODEC_HP_HS4_REF_CONN
- GPIO_ALS_C4_TO_SOC_IRQ_L
- I2C_ALS_SDA_C4_CONN
- I2C_ALS_SCL_C4_CONN
- GPIO_APANEL_HALL_TO_PMU_IRQ_L
- PP1V8_S2_AJ_HALL_CONN
- PP3V0_C4_ALS_CONN
- CODEC_HP_HS4_CONN
- CODEC_HP_LEFT_CONN
- CODEC_HP_RIGHT_CONN
- CODEC_HP_HEADSET_DET_CONN
- CODEC_HP_HS3_CONN
- CODEC_HP_HS3_REF_CONN
- BOARD_TEMP5_N
- BOARD_TEMP5_P

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-09232	1	SHIELD CAN,MLB,KONA,J207	TOUCH_CAN	CRITICAL	
806-17995	1	SHIELD,MLB,WIFI,YY,J217	WIFI_FENCE	CRITICAL	
806-18102	1	FENCE,MLB,AP,YN,J217	AP_FENCE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR (MLB A BEST)	EEEE_K705	CRITICAL	BEST
825-7691	1	EEEE FOR (MLB A ULTIMATE)	EEEE_LF08	CRITICAL	ULTIMATE
825-7691	1	EEEE FOR (MLB A SUPREME)	EEEE_K70V	CRITICAL	SUPREME
825-7691	1	EEEE FOR (MLB A EXTREME)	EEEE_K70J	CRITICAL	EXTREME

SYNC_MASTER=MLB_B_0.46.0 SYNC_DATE=07/09/2019
PAGE TITLE: BASEBAND UNIQUE

SMT TEST FIXTURE TP

POWER - BUCKS

TP9301 PPVDD_CPU
TP9302 PPVDD_GPU
TP9303 PPVDD_S1_SOC
TP9304 PP1V8_S2
TP9305 PP1V8_SW1
TP9306 PP1V8_EXT_SW1
TP9307 PP1V8_CAM
TP9308 PP1V8_S2_EXT_SW2

TP9311 PP1V1_S2

TP9313 PPVDD_S1_FIXED
TP9316 PP2V63_NAND

TP9319 PPVDD_CPU_SRAM
TP9320 PPVDD_GPU_SRAM
TP9321 PPVDD_ECPU

TP938C PPVDD_S1_DCS
TP938D PPVDD_S1_QL

POWER - LDOS

TP9322 PP3V0_S2_HYDRA
TP9323 PP1V7_S2_VA_VCP
TP9324 PP2V6_REAR_CAM_AF
TP9325 PP3V0_ALS

TP9327 PP3V3_ACC
TP9328 PP3V3_USB
TP9329 PP3V05_S2_MESA
TP9330 PP1V19_FRONT_CAM
TP9331 PP0V9_NAND

TP9333 PP2V9_REAR_CAM
TP9334 PP1V2_SOC
TP9335 PP0V75_S2_AOP
TP9336 PP1V8_S2_MESA

POWER - OTHER

TP9340 PPVCENTER
TP9341 PPVBUS_PROT
TP9342 PPVCC_HIGH
TP9343 PP1V8_ALWAYS

TP9345 PPLED_OUT
TP9346 PPVCC_MAIN
TP9347 PPVCC_MAIN
TP9348 PPBATT_POS_RC
TP934A PP16V0_MESA

POWER - CAMERA (NH)

TP9352 PP2V9_FRONT_CAM_AVDD

POWER - DISPLAY

TP9360 PPVCC_MAIN_LCD_SW_CONN
TP9361 PPVCC_MAIN_LCD_SW

POWER - BACKLIGHT

TP9362 PPLED_BACK_REG_A
TP9368 PPLED_BACK_REG_A

TP9363 LED_IO_1_A
TP9364 LED_IO_2_A
TP9365 LED_IO_3_A
TP9366 LED_IO_4_A
TP9367 LED_IO_5_A
TP9374 LED_IO_6_A

TP9369 LED_IO_1_B
TP9370 LED_IO_2_B
TP9371 LED_IO_3_B
TP9372 LED_IO_4_B
TP9373 LED_IO_5_B

TP9375 WLED_LX_A
TP9376 WLED_LX_B

BATTERY

TP9381 BATT_NTC_POS
TP9382 BATT_SNS

HYDRA

TP938A GPIO_HYDRA_TO_SMC_IRQ
TP938B RESET_HYDRA_TO_PMU

USBPD

TP938E PPVDD_USBPD_DET
TP938F CCG2_VBUS_DET

TP9390 PLACE_NEAR=J3700.19:20MM TP-1P0-TOP
TP9391 PLACE_NEAR=J3700.19:20MM TP-1P0-TOP
TP9392 PLACE_NEAR=J3700.19:20MM TP-1P0-TOP PPVBUS_USB_EMI
TP9394 PLACE_NEAR=J3700.9:30MM TP-1P0-TOP
TP9396 PLACE_NEAR=J8900.4:15MM TP-1P0-TOP
TP9397 PLACE_NEAR=J8900.4:15MM TP-1P0-TOP
TP9398 PLACE_NEAR=J8900.4:15MM TP-1P0-TOP

PMU

TP93A0 GPIO_WLAN_TO_PMU_HOST_WAKE
TP93A2 NC_PCIE_BB_TO_APPMU_WAKE_L
TP93A3 ATLAS_TCAL
TP93A5 BOARD_TEMP2_P
TP93A6 BOARD_TEMP3_P
TP93A7 BOARD_TEMP4_P
TP93A8 BOARD_TEMP5_P
TP93A9 BOARD_TEMP6_P
TP93B0 BOARD_TEMP7_P
TP93B1 BOARD_TEMP8_P

TP93B4 TP_AMUX_AY
TP93B5 TP_AMUX_BY

TP93B7 NUB_SPMI_ATLAS_SDATA
TP93B8 NUB_SPMI_ATLAS_SCLK
TP93B9 GPIO_PMU_TO_CPU_TRIGGER_0
TP93BA GPIO_PMU_TO_CPU_TRIGGER_1
TP93BB VCCMAIN_DROOP_PMU_TO_SOC_L
TP93BC SOCHOT1_SOC_TO_PMU_L
TP93BD PMU_SHUTDOWN
TP93BE GPIO_PMU_TO_GPU_TRIGGER_0
TP93BF GPIO_PMU_TO_GPU_TRIGGER_1

TP93BI GPIO_PMU_TO_SOC_BTN_HOME_L
TP93BJ GPIO_PMU_TO_SOC_BTN_ONOFF_L

SOC - JTAG/RESET

TP93C1 JTAG_SOC_SEL
TP93C2 JTAG_SOC_TCK
TP93C3 JTAG_SOC_TMS
TP93C4 JTAG_SOC_TDI
TP93C5 JTAG_SOC_TRST_L
TP93C6 JTAG_SOC_TDO
TP93C7 SOC_TESTMODE
TP93C8 RESET_PMU_TO_SYSTEM_L
TP93C9 GPIO_FORCE_DFU
TP93CA TP_SOC_DFU_STATUS

TP93CB TST_CLKOUT
TP93CC GPIO_PMU_TO_SYSTEM_ACTIVE_READY

SOC - UART

TP93D0 UART_SOC_TO_DEBUG_TX
TP93D1 UART_DEBUG_TO_SOC_TX

SOC - USB

TP93D2 USB_SOC_N
TP93D3 USB_SOC_P

E75

TP93D4 HYDRA_E75_ACC_DET_L
TP93D5 PPVBUS_E75_USB_CONN
TP93D6 PPOUT_E75_ACC_ID1_CONN
TP93D7 PPOUT_E75_ACC_ID2_CONN
TP93D8 E75_DPAIR1_N
TP93D9 E75_DPAIR1_P
TP93E0 E75_DPAIR2_N
TP93E1 E75_DPAIR2_P
TP93EB PPVBUS_USB_EMI

TP93E2 E75_RVP_G
TP93E3 E75_TR_B

TP93EC PPOUT_E75_ACC_ID1_CONN
TP93ED PPOUT_E75_ACC_ID2_CONN

AUDIO - HEADPHONE

TP93E5 CODEC_HP_HEADSET_DET_CONN
TP93E6 CODEC_HP_HS3_CONN
TP93E7 CODEC_HP_HS3_REF_CONN
TP93E8 CODEC_HP_HS4_CONN
TP93E9 CODEC_HP_HS4_REF_CONN
TP93F0 CODEC_HP_LEFT_CONN
TP93F1 CODEC_HP_RIGHT_CONN

AUDIO - SPEAKER AMPS

TP93F2 PPVBOOST_R_CN
TP93F3 PPVBOOST_L_CN

TP93EA GPIO_SPKRAMP_TO_SOC_IRQ_L
TP93FB TDM_SPKRAMP_TO_SPKRAMP_TCC

AUDIO - CODEC

TP93F6 GPIO_CODEC_TO_PMU_WAKE_L

TP93F8 MIKEY_HYDRA_P
TP93F9 MIKEY_HYDRA_N

POWER - SENSORS

TP93GO PP1V8_S2_KOBOL_FILT
TP93G2 PP1V8_PHOS_FILT

I2C

TP93GG I2C1_SCL_1V8
TP93GH I2C1_SDA_1V8
TP93GC I2C2_SCL_1V8
TP93GD I2C2_SDA_1V8
TP93GE I2C3_SCL_1V8
TP93GF I2C3_SDA_1V8
TP93HE I2C4_SCL_1V8
TP93HF I2C4_SDA_1V8

WIFI/BT

TP93I0 GPIO_PMU_TO_BT_REG_ON
TP93I1 GPIO_PMU_TO_WLAN_REG_ON
TP93I2 CLK_PMU_TO_WLAN_32K

TP93IB GPIO_WLAN_TO_SOC_TIME_SYNC
TP93IC JTAG_WLAN_SEL

TP93IE GPIO_AOP_TO_WLAN_CONTEXT_A
TP93IF GPIO_AOP_TO_WLAN_CONTEXT_B

CAMERA - NH

TP93I3 CLK_SOC_TO_FRONT_CAM_12MHZ
TP93I4 ISP_I2C2_SCL_1V8
TP93I5 ISP_I2C2_SDA_1V8
TP93I6 GPIO_SOC_TO_FRONT_CAM_SHTDWN_L

CAMERA - ARIZONA

TP93J3 GPIO_SOC_TO_MINION_CRESET_L
TP93J4 MINION_SPI_MOSI
TP93J2 MINION_SPI_MISO
TP93JA MINION_SPI_SCLK
TP93JB MINION_SPI_CS_L
TP93JE GPIO_FLASH_WP_L
TP93JF GPIO_FLASH_HOLD_L

TP93JG GPIO_MINION_TO_SOC_CONFIG_DONE

MESA

TP93J1 GPIO_MESA_TO_SOC_IRQ
TP93JC PP16V0_MESA
TP93JD GPIO_MESA_TO_BOOST_ENABLE

ALS

TP93J7 GPIO_ALS_C4_TO_SOC_IRQ_L
TP93J8 GPIO_ALS_C3_TO_SOC_IRQ_L

DISPLAY

TP93J9 LPDP_TCON_TO_SOC_HPD
TP93K0 GPIO_PMU_TO_LCD_PWREN

AOP

TP93K1 CLK_PMU_TO_AOP_32K

AUDIO - DIGITAL MICS

TP93K2 DMIC1_MIC_SCLK_CONN
TP93K3 DMIC1_MIC_SD_CONN

AUDIO- BELFIELD

TP93R0 GPIO_BELFIELD_TO_PMU_WAKE_L
TP93R1 GPIO_BELFIELD_TO_SOC_IRQ_L

TOUCH

TP93N1 PP15V0_TOUCH_FILT
TP93N2 PP2V8_KONA_M_VDDANA

TP93N4 KONA_BOOST_VBAT
TP93N5 KONA_BOOST_EN

SOC - ACC UART

TP93N8 UART_SOC_TO_ACC_TX
TP93N9 UART_ACC_TO_SOC_TX

SOC - GND

TP93NA SOC_SENSE_NEG
TP93NB CPU_PCORE_SENSE_NEG
TP93NF VDDQL_DCS_SENSE_NEG

SOC - POWER

TP93NC ADC_SOC_TO_PMU_VDD_CPU
TP93ND ADC_SOC_TO_PMU_VDD_GPU
TP93NE ADC_SOC_TO_PMU_VDD_SOC

PLACE VSS SENSE TEST POINTS NEAR BY

SMC I2C

TP93GK I2C_SMC_I2CM0_SCL_1V8
TP93GL I2C_SMC_I2CM0_SDA_1V8
TP93GM I2C_SMC_I2CM1_SCL_1V8
TP93GN I2C_SMC_I2CM1_SDA_1V8

USB

TP93HC PLACE_NEAR=U3512.5:1MM USB_KIS_P
TP93HD PLACE_NEAR=U3512.4:1MM USB_KIS_N

TP93GO
TP93GP
TP93GQ
TP93GR
TP93GS
TP93GT
TP93KU
TP93GV

SYNC_MASTER=J217_MLB_B
SYNC_DATE=10/01/2018
PAGE TITLE
TEST: TPS/HOLES/FIDUCUALS

EE CHARACTERIZATION PP/TP

SOC

PP9504 P3MM SM (PP) 1 ADC SOC TO PMU ANALOGMUX OUT — 5 39
PP950C P3MM SM (PP) 1 VDDQL SENSE POS — 13
PP9505 P3MM SM (PP) 1 ADC SOC TO PMU VDD SOC — 13 39 47
PP9506 P3MM SM (PP) 1 SOC SENSE NEG — 13 47
PP9507 P3MM SM (PP) 1 ADC SOC TO PMU VDD GPU — 13 37 39 47
PP9508 P3MM SM (PP) 1 GPU SENSE NEG — 13
PP9509 P3MM SM (PP) 1 DCS SENSE POS — 13
PP950A P3MM SM (PP) 1 ADC SOC TO PMU VDD CPU — 13 37 39 47
PP950B P3MM SM (PP) 1 CPU PCORE SENSE NEG — 13 47
PP950E P3MM SM (PP) 1 PP SOC DEBUG2 — 7
PP950F P3MM SM (PP) 1 PP SOC DEBUG3 — 7
PP950G P2MM SM (PP) 1 PP SOC AON SLEEP1 RESET L — 11

HYDRA

PP9503 P2MM SM (PP) 1 TP HYDRA EXT SW EN — 27

CODEC I2S

PP9510 P2MM SM (PP) 1 I2S AOP TO CODEC BCLK — 11 24
PP9511 P2MM SM 1 I2S AOP TO CODEC LRCK — 11 24
PP9512 P2MM SM (PP) 1 I2S AOP TO CODEC DOUT — 11 24
PP9513 P2MM SM (PP) 1 I2S CODEC TO AOP DOUT — 11 24

BELFIELD I2S

PP9514 P2MM SM (PP) 1 I2S0 SOC TO BELFIELD BCLK — 9 24
PP9515 P2MM SM (PP) 1 I2S0 SOC TO BELFIELD LRCK — 9 24
PP9516 P2MM SM 1 I2S0 SOC TO BELFIELD DOUT — 9 24
PP9517 P2MM SM (PP) 1 I2S0 BELFIELD TO SOC DOUT — 9 24
PP9518 P2MM SM (PP) 1 I2S0 SOC TO BELFIELD MCLK — 9 24

CN SPEAKER I2S

PP9525 P2MM SM (PP) 1 I2S1 SOC TO SPKRAMP CN MCLK — 9 26
PP9526 P2MM SM (PP) 1 I2S1 SOC TO SPKRAMP CN BCLK — 9 26
PP9527 P2MM SM (PP) 1 I2S1 SOC TO SPKRAMP CN LRCK — 9 26
PP9528 P2MM SM (PP) 1 I2S1 SOC TO SPKRAMP CN DOUT — 9 26
PP9529 P2MM SM (PP) 1 I2S1 SPKRAMP CN TO SOC DOUT — 9 26

POTOMAC

PP9539 P2MM SM (PP) 1 SYS ALIVE — 16 39

AUDIO

PP953A P2MM SM (PP) 1 GPIO CODEC TO SOC IRQ L — 9 24

BELFIELD SPI LINES

PP9540 P3MM SM (PP) 1 SPI BELFIELD CS L — 9 24
PP9542 P3MM SM (PP) 1 SPI BELFIELD MOSI — 9 24
PP9543 P3MM SM (PP) 1 SPI BELFIELD MISO — 9 24

SENSOR SPI LINES

PP9544 P3MM SM (PP) 1 SPI SENSORS SCLK — PLACE_NEAR=U2150.2.10MM — 11 17 25 48
PP9545 P3MM SM (PP) 1 SPI SENSORS MISO — PLACE_NEAR=U2150.3.10MM — 11 17 25 48
PP9546 P3MM SM (PP) 1 SPI SENSORS MOSI — PLACE_NEAR=U2150.3.10MM — 11 17 25 48
PP9547 P3MM SM (PP) 1 SPI SENSORS SCLK — PLACE_NEAR=U2120.4.10MM — 11 17 25 48
PP9548 P3MM SM (PP) 1 SPI SENSORS SCLK — PLACE_NEAR=U2140.A3.10MM — 11 17 25 48
PP9549 P3MM SM (PP) 1 SPI SENSORS MOSI — PLACE_NEAR=U2120.3.10MM — 11 17 25 48
PP954A P3MM SM (PP) 1 SPI SENSORS MOSI — PLACE_NEAR=U2140.A4.10MM — 11 17 25 48

MESA SPI LINES

PP954B P3MM SM (PP) 1 SPI MESA MISO — 9 31
PP954C P3MM SM (PP) 1 SPI MESA MOSI CONN — 29 31
PP954D P3MM SM (PP) 1 SPI MESA SCLK CONN — 29 31

CAMERA - FRONT

PP9560 P2MM SM (PP) 1 MIPI NH CAM TO SOC CLK P — NO_XNET_CONNECTION=1 — 7 23
PP9561 P2MM SM (PP) 1 MIPI NH CAM TO SOC CLK N — NO_XNET_CONNECTION=1 — 7 23
PP9562 P2MM SM (PP) 1 MIPI NH CAM TO SOC DATA P<0> — NO_XNET_CONNECTION=1 — 7 23
PP9563 P2MM SM (PP) 1 MIPI NH CAM TO SOC DATA N<0> — NO_XNET_CONNECTION=1 — 7 23
PP9564 P2MM SM (PP) 1 MIPI NH CAM TO SOC DATA P<1> — NO_XNET_CONNECTION=1 — 7 23
PP9565 P2MM SM (PP) 1 MIPI NH CAM TO SOC DATA N<1> — NO_XNET_CONNECTION=1 — 7 23

CAMERA - REAR & MINION

PP9566 P2MM SM (PP) 1 MIPI MINION TO SOC CLK P — NO_XNET_CONNECTION=1 — 7 21
PP9567 P2MM SM 1 MIPI MINION TO SOC CLK N — NO_XNET_CONNECTION=1 — 7 21
PP9568 P2MM SM (PP) 1 MIPI MINION TO SOC DATA P<0> — NO_XNET_CONNECTION=1 — 7 21
PP9569 P2MM SM (PP) 1 MIPI MINION TO SOC DATA N<0> — NO_XNET_CONNECTION=1 — 7 21
PP956G P2MM SM (PP) 1 MIPI MINION TO SOC DATA P<1> — NO_XNET_CONNECTION=1 — 7 21
PP956H P2MM SM (PP) 1 MIPI MINION TO SOC DATA N<1> — NO_XNET_CONNECTION=1 — 7 21

PP956A P2MM SM (PP) 1 MIPI CAM REAR TO MINION CLK P — NO_XNET_CONNECTION=1 — 21 46
PP956B P2MM SM (PP) 1 MIPI CAM REAR TO MINION CLK N — NO_XNET_CONNECTION=1 — 21 46
PP956C P2MM SM (PP) 1 MIPI CAM REAR TO MINION DATA P<0> — NO_XNET_CONNECTION=1 — 21 46
PP956D P2MM SM (PP) 1 MIPI CAM REAR TO MINION DATA N<0> — NO_XNET_CONNECTION=1 — 21 46
PP956E P2MM SM (PP) 1 GPIO MINION TO SOC CONFIG DONE — NO_XNET_CONNECTION=1 — 7 21 47
PP956F P2MM SM (PP) 1 CLK SOC TO MINION 12MHZ — NO_XNET_CONNECTION=1 — 7 21

GRAPE

PP9580 P2MM SM (PP) 1 SPI SOC TO GRAPE SCLK — 9 18
PP9581 P3MM SM (PP) 1 SPI SOC TO GRAPE MISO — 9 18
PP9582 P3MM SM (PP) 1 SPI SOC TO GRAPE MOSI — 9 18
PP9583 P3MM SM (PP) 1 SPI SOC TO GRAPE CS L — 9 18
PP9584 P3MM SM (PP) 1 GPIO SOC TO GRAPE RESET L — 10 18 19
PP9585 P3MM SM (PP) 1 GPIO GRAPE TO SOC IRQ L — 10 18

PP958C P3MM SM (PP) 1 KONA BOOST ATEST — 18

PP958L P3MM SM (PP) 1 TP KONA GPIO ADC 03 — 18
PP958M P3MM SM (PP) 1 CLK KONA M 24MHZ — 18
PP958N P3MM SM (PP) 1 GPIO SOC TO GRAPE BSYNC0 — 18 19 29
PP958P P3MM SM (PP) 1 GPIO SOC TO GRAPE BSYNC1 — 18 19 29

GRAPE POWER

PP958R P3MM SM (PP) 1 PP3V3 GRAPE FILT — 19 — 18
PP958S P3MM SM (PP) 1 PP1V8 GRAPE XTAL FILT — 18 19
PP958T P3MM SM (PP) 1 KONA M VDDCORE CAP — 18

PP958V P3MM SM (PP) 1 PP1V8 GRAPE AON RC — 18 19

NAND PCIE TPS

PP95D4 P2MM SM (PP) 1 PLACE_NEAR=U1700.K11:3MM — PCIE SOC TO NAND1 REFCLK P — 6 16
PP95D5 P2MM SM (PP) 1 PLACE_NEAR=U1700.J12:3MM — PCIE SOC TO NAND1 REFCLK N — 6 16
PP95D6 P2MM SM (PP) 1 PLACE_NEAR=U1700.E8:20MM — PCIE SOC TO NAND1 RESET L — 6 16
PP95D7 P2MM SM (PP) 1 PLACE_NEAR=U1700.J4:20MM — NAND1 ANI1 VREF — 16
PP95D8 P2MM SM (PP) 1 PLACE_NEAR=U1700.G12:20MM — NAND1 ANI0 VREF — 16

PP95DI P2MM SM (PP) 1 PLACE_NEAR=U1800.C4:20MM — GPIO SOC TO NAND FW STRAP — 5 16
PP95DJ P2MM SM (PP) 1 PLACE_NEAR=U1800.L4:20MM — GPIO SOC TO NAND RESET L — 5 16

PMU/POTOMAC

PP95G1 P2MM SM (PP) 1 GPIO PMU TO SOC IRQ L — 11 39
PP95G2 P2MM SM (PP) 1 GPIO POTOMAC TO PMU WAKE — 39 40
PP95G3 P2MM SM (PP) 1 GPIO POTOMAC TO SMC TO PMU IRQ L — 9 39 40
PP95G4 P2MM SM (PP) 1 ORION TO POTOMAC OVP SW EN L — 36 40
PP95G5 P2MM SM 1 GPIO PMU TO POTOMAC LINCH EN — 39 40
PP95G6 P2MM SM (PP) 1 ATLAS FAULT OUT L — 39
PP95G7 P2MM SM (PP) 1 USB VBUS DETECT — 5 40

WIFI

PP95BL P2MM SM (PP) 1 GPIO SOC TO BT TO GRAPE TS SYNC — 10 18 19 32 33 45
PP95BM P2MM SM (PP) 1 GPIO TOUCH TO BT SYNC — 18 32 33 45

WLAN PCIE TPS

PP95E0 P2MM SM (PP) 1 PLACE_NEAR=U0600.BE11:3MM — PCIE WLAN TO SOC TX P — 6 45
PP95E1 P2MM SM (PP) 1 PLACE_NEAR=U0600.BE11:3MM — PCIE WLAN TO SOC TX N — 6 45
PP95E2 P2MM SM (PP) 1 PLACE_NEAR=U0600.BF39:4MM — PCIE WLAN TO SOC CLKREQ L — 6 45

PP95E7 P2MM SM (PP) PLACE_NEAR=U4900.67:3MM — PCIE SOC TO WLAN RESET L — 6 45

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POWER CONNECTIONS

BUCK0 (ACTIVE)

PPVDD_CPU — MAKE_BASE=TRUE
- 47 37 PPVDD_CPU
- 12 15 37 PPVDD_CPU

BUCK1 (SW CONTROL)

PPVDD_GPU — MAKE_BASE=TRUE
- 47 37 PPVDD_GPU
- 12 15 37 PPVDD_GPU

BUCK2 (SLEEP1)

PPVDD_S1_SOC — MAKE_BASE=TRUE
- 47 37 PPVDD_S1_SOC
- 12 15 36 PPVDD_S1_SOC

BUCK3 (SLEEP2)

PP1V8_S2 — MAKE_BASE=TRUE
- 47 37 36 5 PP1V8_S2
- 13 PP1V8_S2
- 27 PP1V8_S2
- 22 25 39 PP1V8_S2
- 41 PP1V8_S2
- 38 PP1V8_S2
- 38 PP1V8_S2
- 11 13 36 PP1V8_S2
- 9 30 39 43 44 PP1V8_S2
- 11 42 PP1V8_S2

BUCK3 INTERNAL SWITCHES

BUCK3_SW1 (ACTIVE)

PP1V8_SW1 — MAKE_BASE=TRUE
- 47 38 PP1V8_SW1
- 26 PP1V8_SW1
- 40 44 PP1V8_SW1

BUCK3_SW2 (SW CONTROL)

PP1V8_GRAPE — MAKE_BASE=TRUE
- 38 36 PP1V8_GRAPE
- 11 18 19 PP1V8_GRAPE

BUCK3_SW3 (SLEEP2)

PP1V8_S2_SENSOR — MAKE_BASE=TRUE
- 38 PP1V8_S2_SENSOR
- 17 PP1V8_S2_SENSOR
- 17 PP1V8_S2_SENSOR
- 25 PP1V8_S2_SENSOR

BUCK3 EXTERNAL SWITCHES

BUCK3_EXT_SW1 (ACTIVE)

PP1V8_EXT_SW1 — MAKE_BASE=TRUE
- 47 41 PP1V8_EXT_SW1
- 13 PP1V8_EXT_SW1
- 5 PP1V8_EXT_SW1
- 7 PP1V8_EXT_SW1
- 5 46 PP1V8_EXT_SW1
- 11 16 36 PP1V8_EXT_SW1
- 9 PP1V8_EXT_SW1
- 4 5 6 9 36 39 46 PP1V8_EXT_SW1
- 13 PP1V8_EXT_SW1
- 38 PP1V8_EXT_SW1

BUCK3_S2_EXT_SW2 (SLEEP2)

PP1V8_S2_EXT_SW2 — MAKE_BASE=TRUE
- 47 41 PP1V8_S2_EXT_SW2
- 45 PP1V8_S2_EXT_SW2
- 45 PP1V8_S2_EXT_SW2
- 24 PP1V8_S2_EXT_SW2
- 25 PP1V8_S2_EXT_SW2

BUCK4 (SLEEP2)

PP1V1_S2 — MAKE_BASE=TRUE
- 47 37 PP1V1_S2
- 38 PP1V1_S2
- 13 36 PP1V1_S2

BUCK5 (SLEEP1)

PPVDD_S1_FIXED — MAKE_BASE=TRUE
- 47 37 PPVDD_S1_FIXED
- 13 36 PPVDD_S1_FIXED
- 6 12 36 PPVDD_S1_FIXED
- 7 36 PPVDD_S1_FIXED
- 12 15 PPVDD_S1_FIXED
- 5 PPVDD_S1_FIXED
- 8 36 PPVDD_S1_FIXED
- 12 PPVDD_S1_FIXED
- 12 PPVDD_S1_FIXED
- 12 PPVDD_S1_FIXED

BUCK6 (ACTIVE)

PP2V63_NAND — MAKE_BASE=TRUE
- 47 37 PP2V63_NAND
- 16 36 PP2V63_NAND

BUCK7 (ACTIVE)

PPVDD_CPU_SRAM — MAKE_BASE=TRUE
- 37 PPVDD_CPU_SRAM
- 12 15 PPVDD_CPU_SRAM

BUCK8 (SW CONTROL)

PPVDD_GPU_SRAM — MAKE_BASE=TRUE
- 47 37 PPVDD_GPU_SRAM
- 12 15 PPVDD_GPU_SRAM

BUCK9 (SLEEP1)

PPVDD_S1_DCS — MAKE_BASE=TRUE
- 37 PPVDD_S1_DCS
- 13 PPVDD_S1_DCS

BUCK10 (SLEEP1)

PPVDD_S1_QL — MAKE_BASE=TRUE
- 47 37 PPVDD_S1_QL
- 13 15 46 PPVDD_S1_QL

BUCK11 (ACTIVE)

PPVDD_ECPU — MAKE_BASE=TRUE
- 37 PPVDD_ECPU
- 12 15 PPVDD_ECPU

LDO1 (SLEEP2)

PP3V0_S2_HYDRA — MAKE_BASE=TRUE
- 38 PP3V0_S2_HYDRA
- 27 PP3V0_S2_HYDRA
- 42 PP3V0_S2_HYDRA

LDO2 (S2 - LDO MODE)

PP1V7_S2_VA_VCP — MAKE_BASE=TRUE
- 47 38 PP1V7_S2_VA_VCP
- 24 PP1V7_S2_VA_VCP
- 38

LDO3 (SW CONTROL)

PP1V8_CAM — MAKE_BASE=TRUE
- 47 38 7 PP1V8_CAM
- 23 PP1V8_CAM
- 21 22 PP1V8_CAM

LDO4 (SW CONTROL)

PP3V0_ALS — MAKE_BASE=TRUE
- 38 PP3V0_ALS
- 22 PP3V0_ALS
- 25 PP3V0_ALS

LDO5 (ACTIVE)

PP3V3_GRAPE — MAKE_BASE=TRUE
- 38 36 PP3V3_GRAPE
- 18 PP3V3_GRAPE

LDO6 (SW CONTROL)

PP3V3_ACC — MAKE_BASE=TRUE
- 47 38 PP3V3_ACC
- 27 PP3V3_ACC

LDO7 (ACTIVE)

PP3V3_USB — MAKE_BASE=TRUE
- 47 38 PP3V3_USB
- 5 46 PP3V3_USB

LDO8 (SLEEP2)

PP3V05_S2_MESA — MAKE_BASE=TRUE
- 47 38 PP3V05_S2_MESA
- 31 PP3V05_S2_MESA

LDO9 (SPARE)

PP1V19_SPARE_LDO9 — MAKE_BASE=TRUE
- 38 PP1V19_SPARE_LDO9

LDO10 (ACTIVE)

PP0V9_NAND — MAKE_BASE=TRUE
- 47 38 PP0V9_NAND
- 16 36 PP0V9_NAND

LDO011 (SW CONTROL)

PP2V9_REAR_CAM — MAKE_BASE=TRUE
- 47 38 PP2V9_REAR_CAM
- 22 PP2V9_REAR_CAM

LDO013 (SW CONTROL)

PP2V9_FRONT_CAM_AVDD — MAKE_BASE=TRUE
- 38 PP2V9_FRONT_CAM_AVDD
- 23 47 PP2V9_FRONT_CAM_AVDD

LDO014 (ACTIVE)

PP1V2_SOC — MAKE_BASE=TRUE
- 47 38 PP1V2_SOC
- 8 PP1V2_SOC
- 12 13 PP1V2_SOC
- 6 PP1V2_SOC

LDO015 (SLEEP2)

PP0V75_S2_AOP — MAKE_BASE=TRUE
- 47 38 PP0V75_S2_AOP
- 12 PP0V75_S2_AOP

LDO016 (SLEEP2)

PP1V8_S2_MESA — MAKE_BASE=TRUE
- 47 38 PP1V8_S2_MESA
- 31 PP1V8_S2_MESA

LDO017 (SW CONTROL)

PP1V19_FRONT_CAM — MAKE_BASE=TRUE
- 47 38 PP1V19_FRONT_CAM
- 23 PP1V19_FRONT_CAM

LDO018 (SW CONTROL)

PP1V25_REAR_CAM — MAKE_BASE=TRUE
- 38 36 PP1V25_REAR_CAM
- 21 22 PP1V25_REAR_CAM

LDO019 (SW CONTROL)

PP2V6_REAR_CAM_AF — MAKE_BASE=TRUE
- 47 PP2V6_REAR_CAM_AF
- 21 22 PP2V6_REAR_CAM_AF

CHARGER MAIN

PPVCC_MAIN — MAKE_BASE=TRUE
- 47 40 36 PPVCC_MAIN
- 37 PPVCC_MAIN
- 37 PPVCC_MAIN
- 37 PPVCC_MAIN
- 37 PPVCC_MAIN
- 24 PPVCC_MAIN
- 39 PPVCC_MAIN
- 36 38 PPVCC_MAIN
- 31 PPVCC_MAIN
- 45 PPVCC_MAIN
- 38 PPVCC_MAIN
- 37 41 PPVCC_MAIN
- 18 PPVCC_MAIN
- 26 PPVCC_MAIN

CHARGER HIGH

PPVCC_HIGH — MAKE_BASE=TRUE
- 47 40 PPVCC_HIGH
- 38 PPVCC_HIGH
- 31 PPVCC_HIGH

BATTERY

PPBATT_VCC — MAKE_BASE=TRUE
- 40 36 PPBATT_VCC
- 43 PPBATT_VCC

USB POWER INPUT

PPVBUS_PROT — MAKE_BASE=TRUE
- 47 PPVBUS_PROT
- 36 40 PPVBUS_PROT

PMU_ON_BUF

PP1V8_ALWAYS — MAKE_BASE=TRUE
- 47 39 PP1V8_ALWAYS
- 39 40 PP1V8_ALWAYS

BACKLIGHT BOOST

PPLED_OUT — MAKE_BASE=TRUE
- 47 39 38 36 PPLED_OUT
- 39 PPLED_OUT

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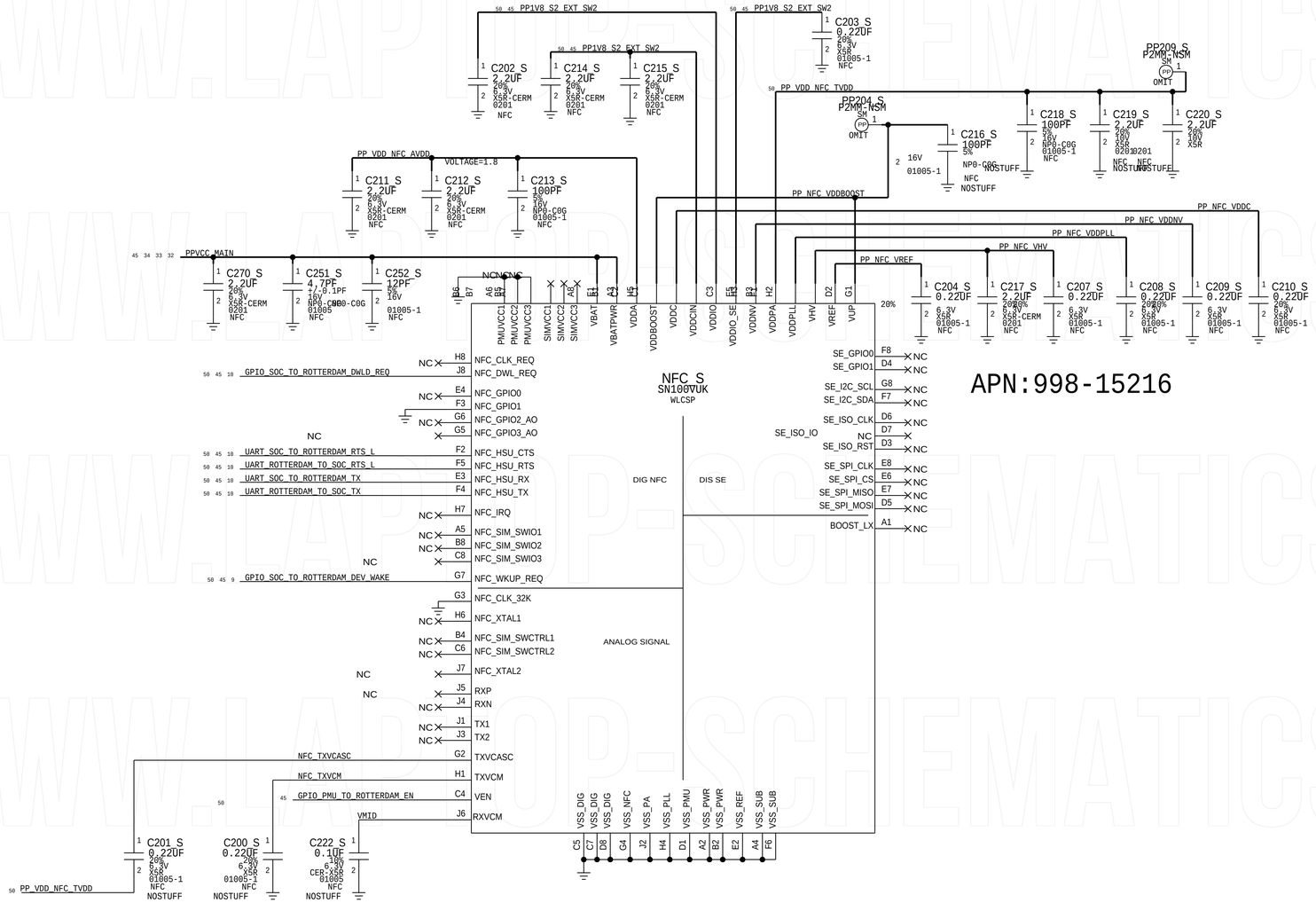
POWER: ALIASES

VENUS



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