

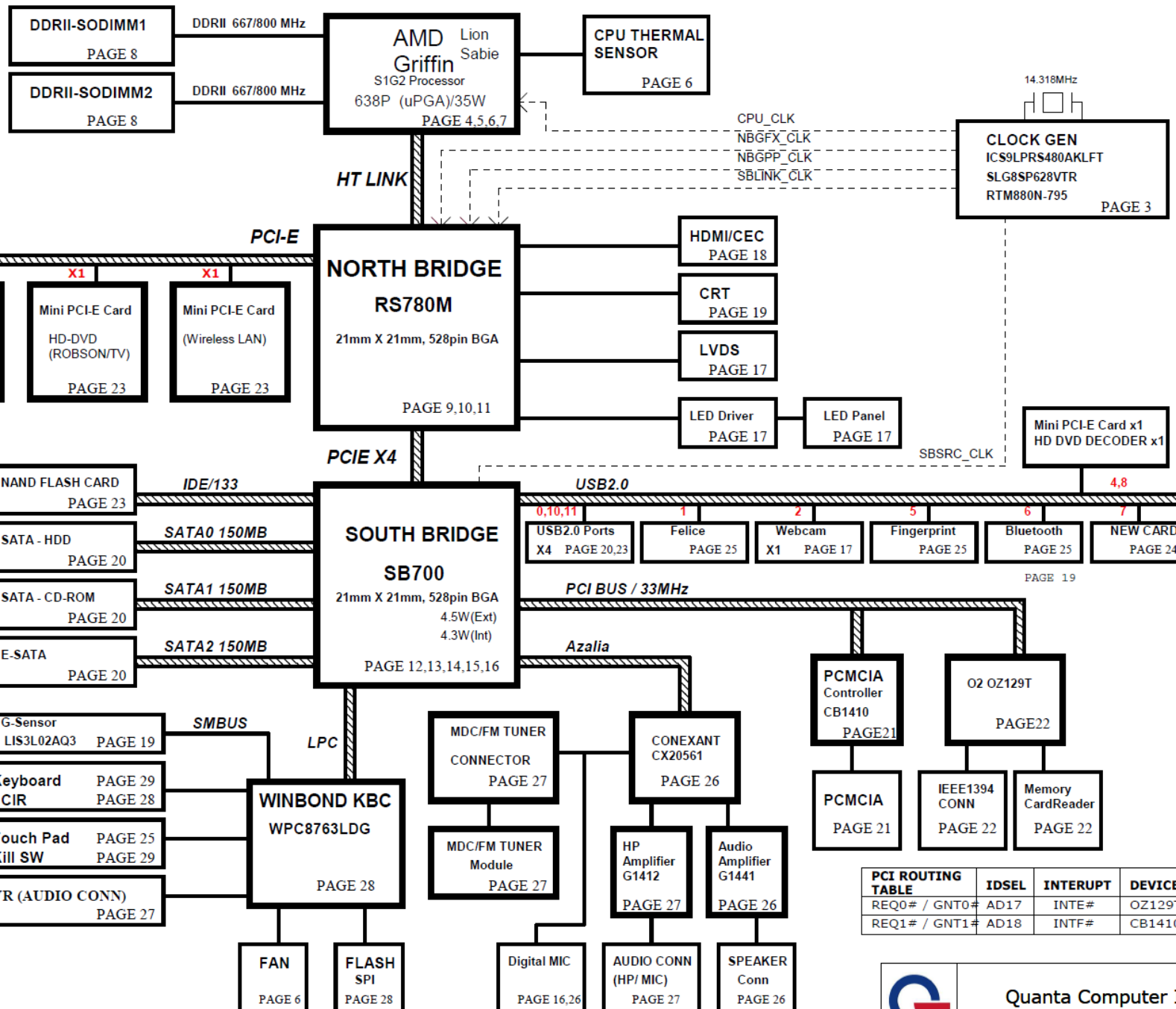
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

BU2G SYSTEM DIAGRAM



01



PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410



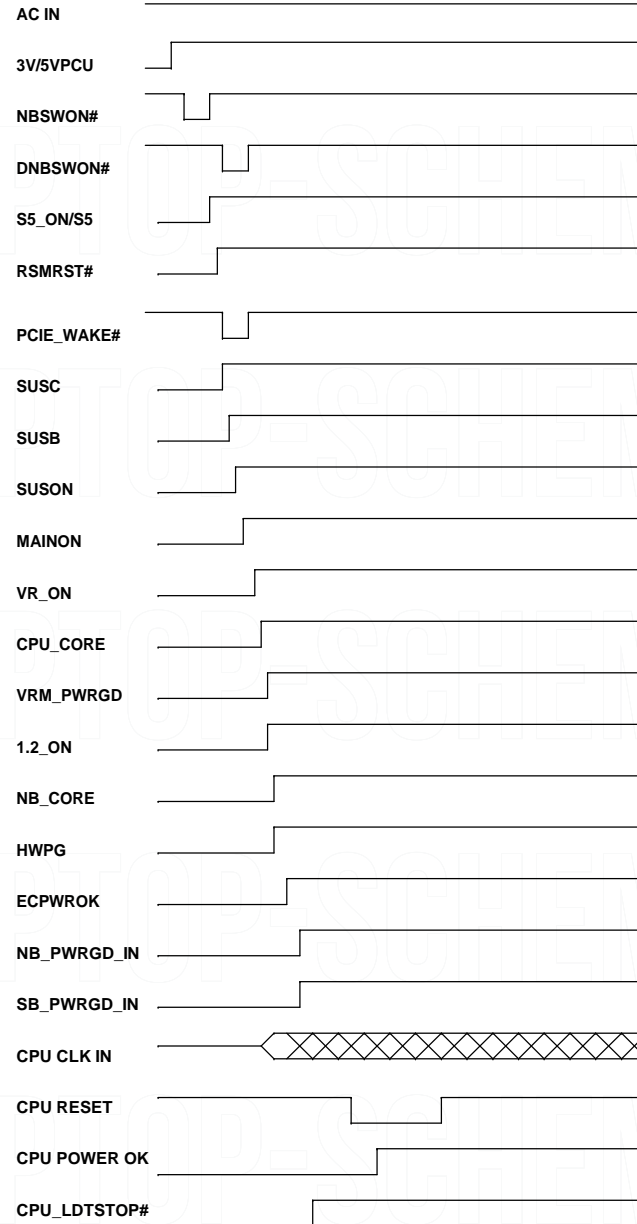
Quanta Computer Inc.

Size Custom Document Number BLOCK DIAGRAM Rev 1A
Date: Wednesday, January 30, 2008 Sheet 1 of 35

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17	LCD/LED PANEL/LID/CAMERA	
18	HDMI/HDMI-CEC(R5F211A)	
19	CRT & G-SENSOR(LIS3L02A)	
20	SATA HDD/ODD & ESATA/USB	
21	PCMCIA(CB1410) -OPTION	
22	OZ129T(5IN1/1394)	
23	MINI CARD & NAND FLASH CARD	
24	NEW CARD & RJ45 BOARD/BEEP	
25	TP/FP/BT/PB/FELICA/MMB CONN	
26	CONEXANT(CX205601)/SPK/AMP	
27	JACK/VR/FM/MIC/MDC/AMPLIFIER	
28	EC(KBC)-WPCPC8763/WPC8769	
29	KEYBOARD/LED/KILL SW/HOLE	
30	CHARGER (ISL6251A)	
31	SYSTEM 5V/3V (ISL6237)	
32	AMD GRIFFIN (ISL6265)	
33	+NB_CORE (RT8202)	
34	DDR 1.8V(TPS51116)	
35	DISCHARGE (1.25V/1.5V)	

Power Sequence



SB700 SM BUS

SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

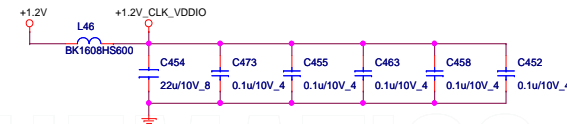
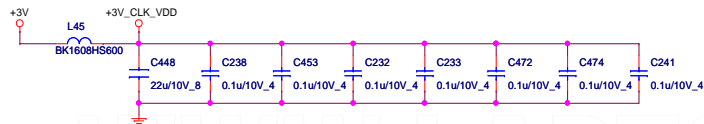
KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)



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Size Custom	Document Number SYSTEM INFORMATION	Rev 1A
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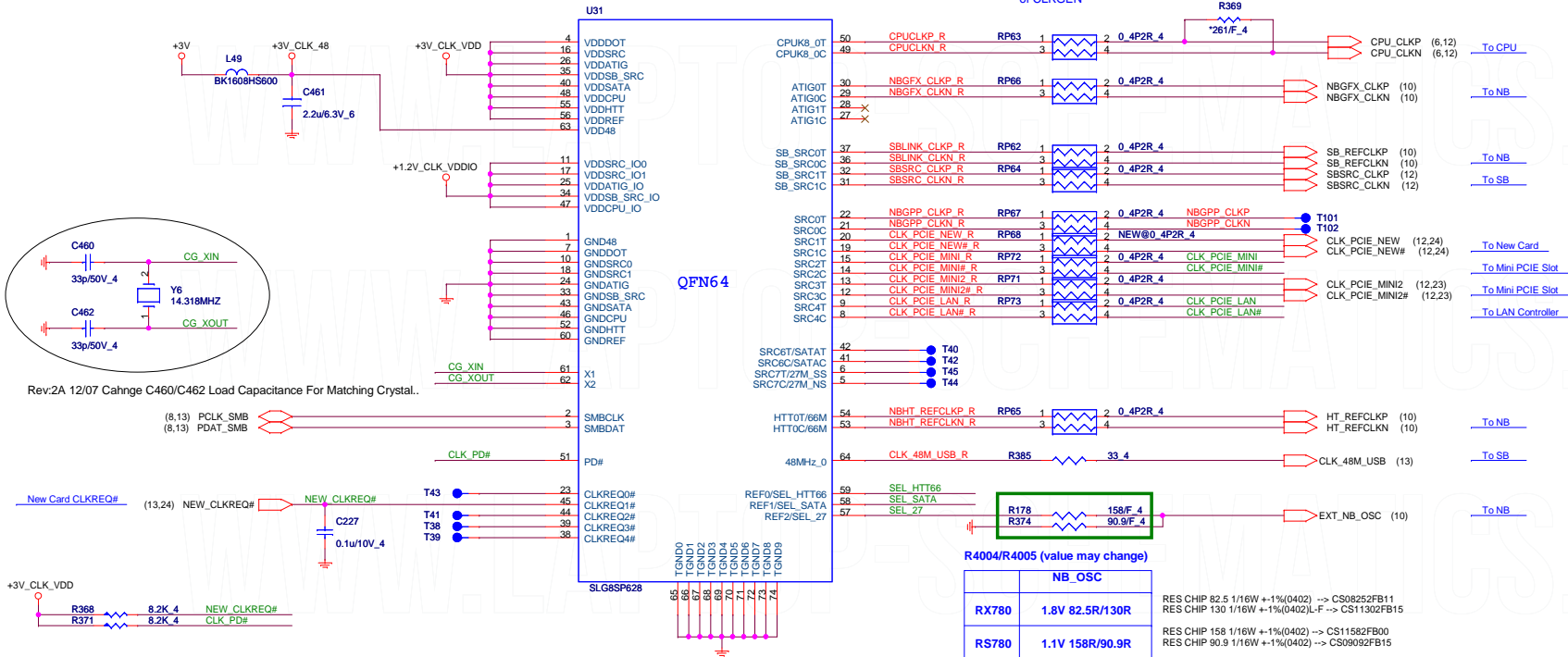


ICS9LPRS480
SLG8SP628
RTM880N-796

P/N :
P/N : AL8SP628000
P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



NB CLOCK INPUT TABLE

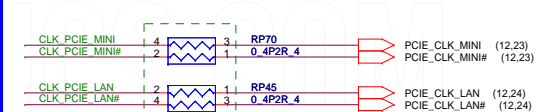
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

R4004/R4005 (value may change)

NB_OSC	
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +1%(0402) -> CS08252FB11
RES CHIP 130 1/16W +1%(0402)L-F -> CS11302FB15
RES CHIP 158 1/16W +1%(0402) -> CS11582FB00
RES CHIP 90.9 1/16W +1%(0402) -> CS09092FB15

FOR EXTERNAL/INTERNAL CLOCK



Place Close to Drivers Side

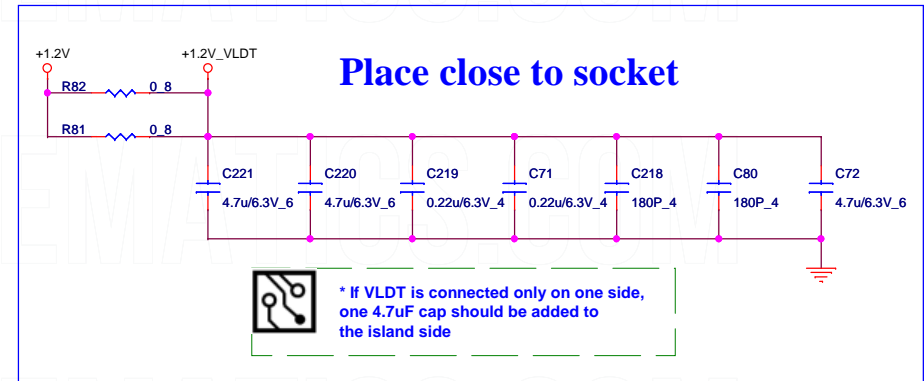
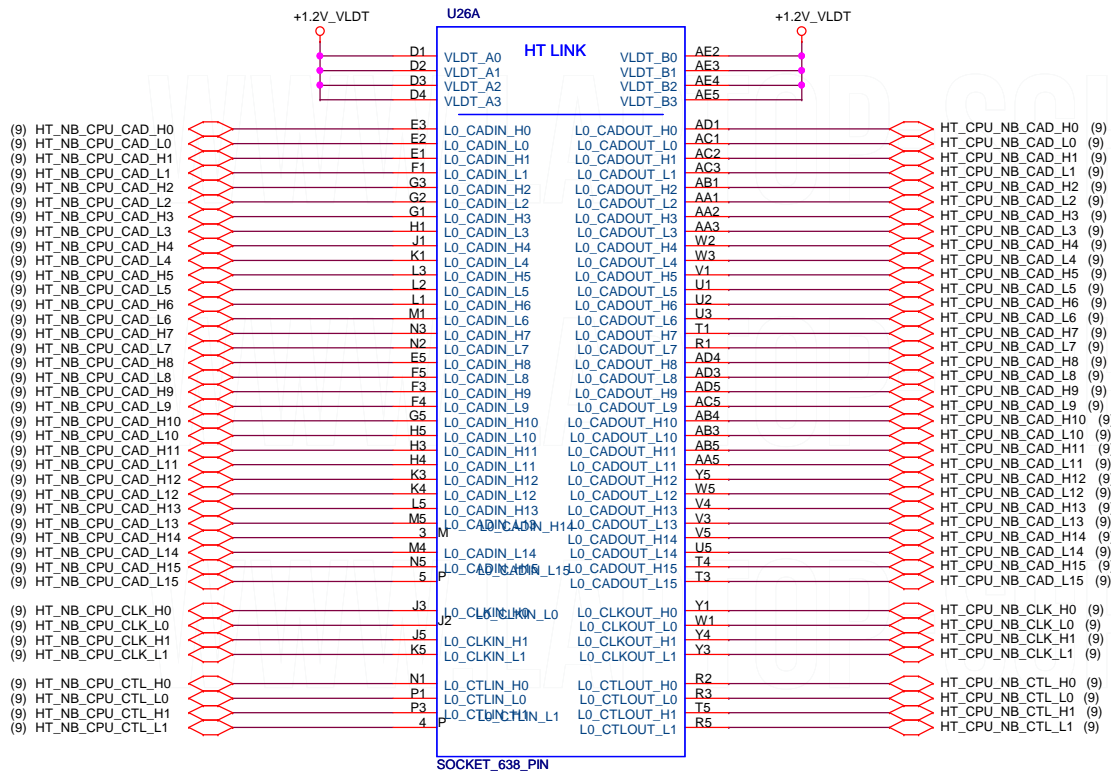
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

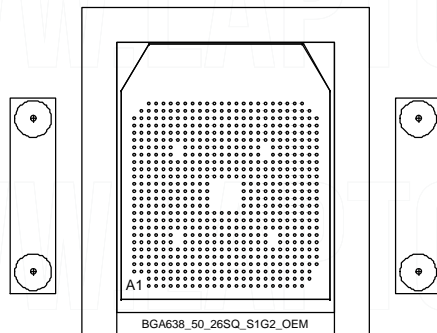


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Size Custom Document Number
CLOCK GENERATOR_SLG8SP628 Rev 1A
Date: Thursday, July 24, 2008 Sheet 3 of 35



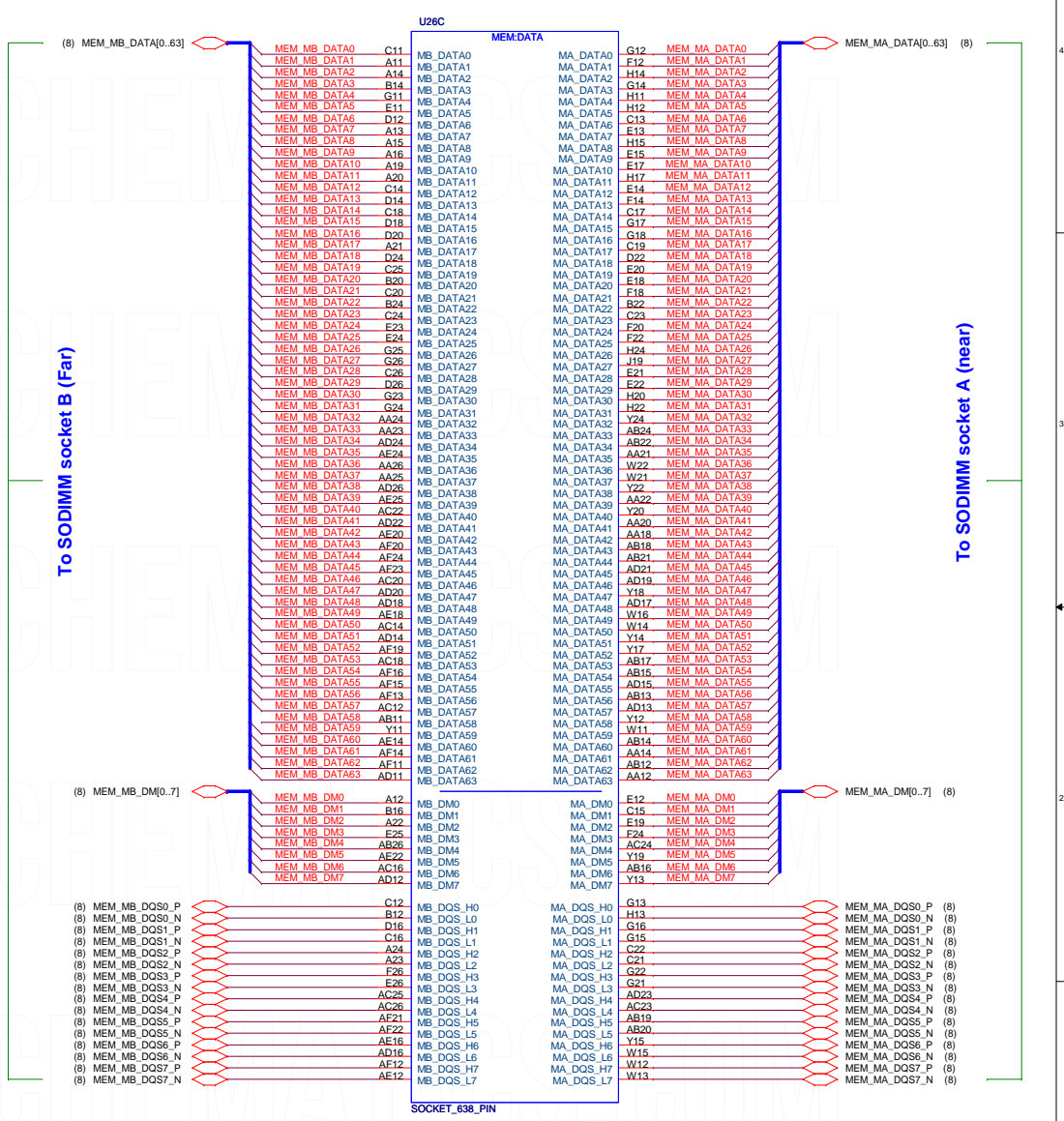
CPU



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Size	Document Number	Rev
B	S1G2 HT I/F 1/4	1A
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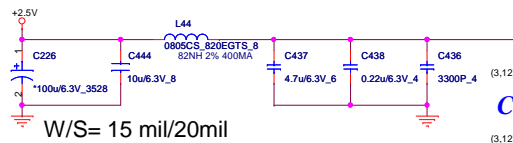
Processor Memory Interface



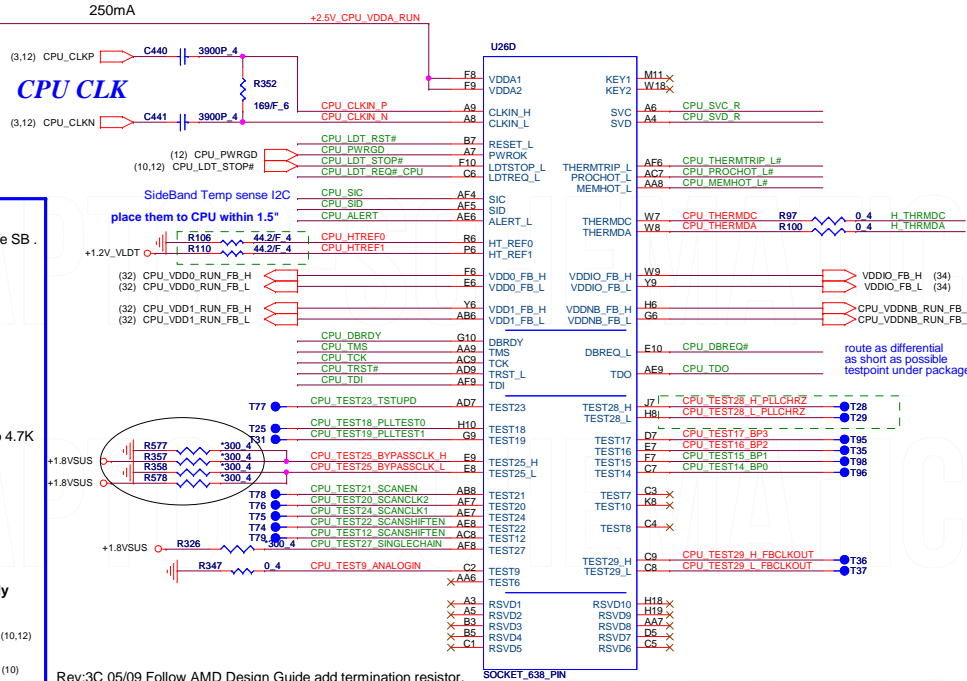
To SODIMM socket A (near)

Place close to socket

CPU

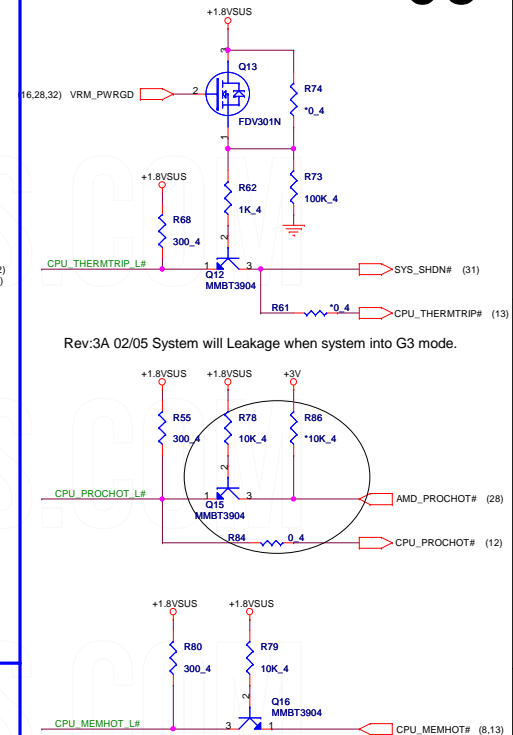


CPU CLK



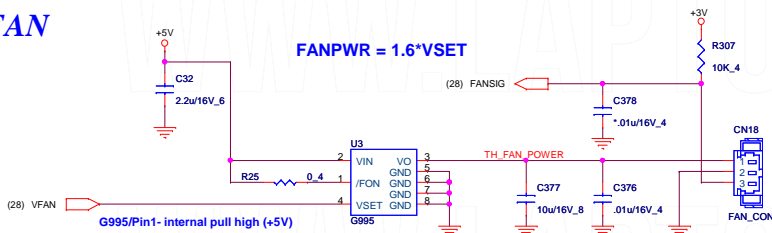
CPU THERM

06

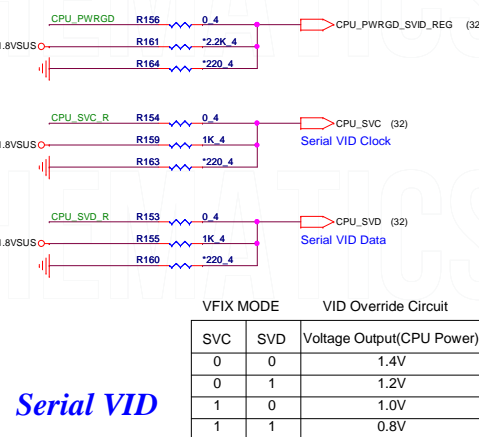
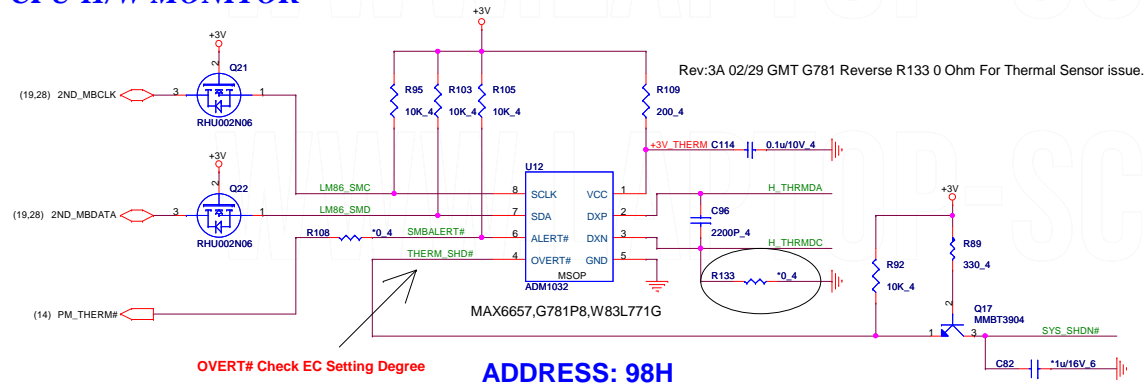


CPU FAN

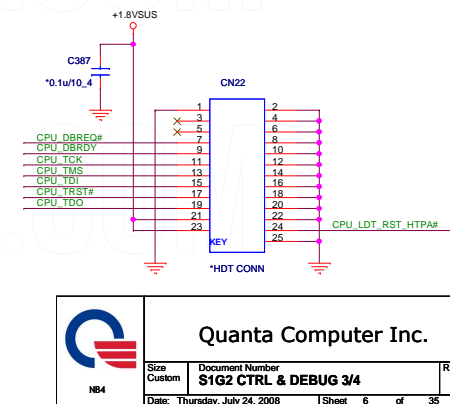
FANPWR = 1.6*VSET



CPU H/W MONITOR

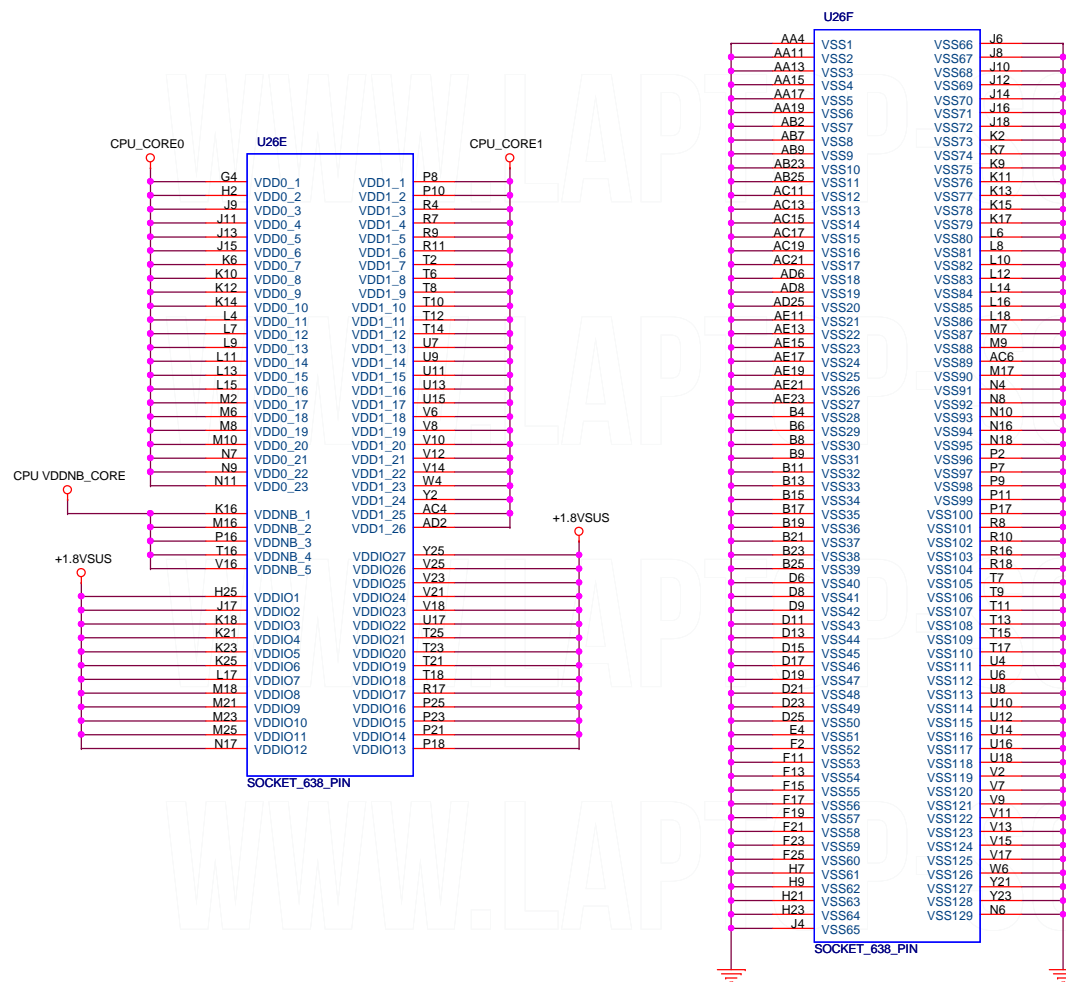


HDT Connector

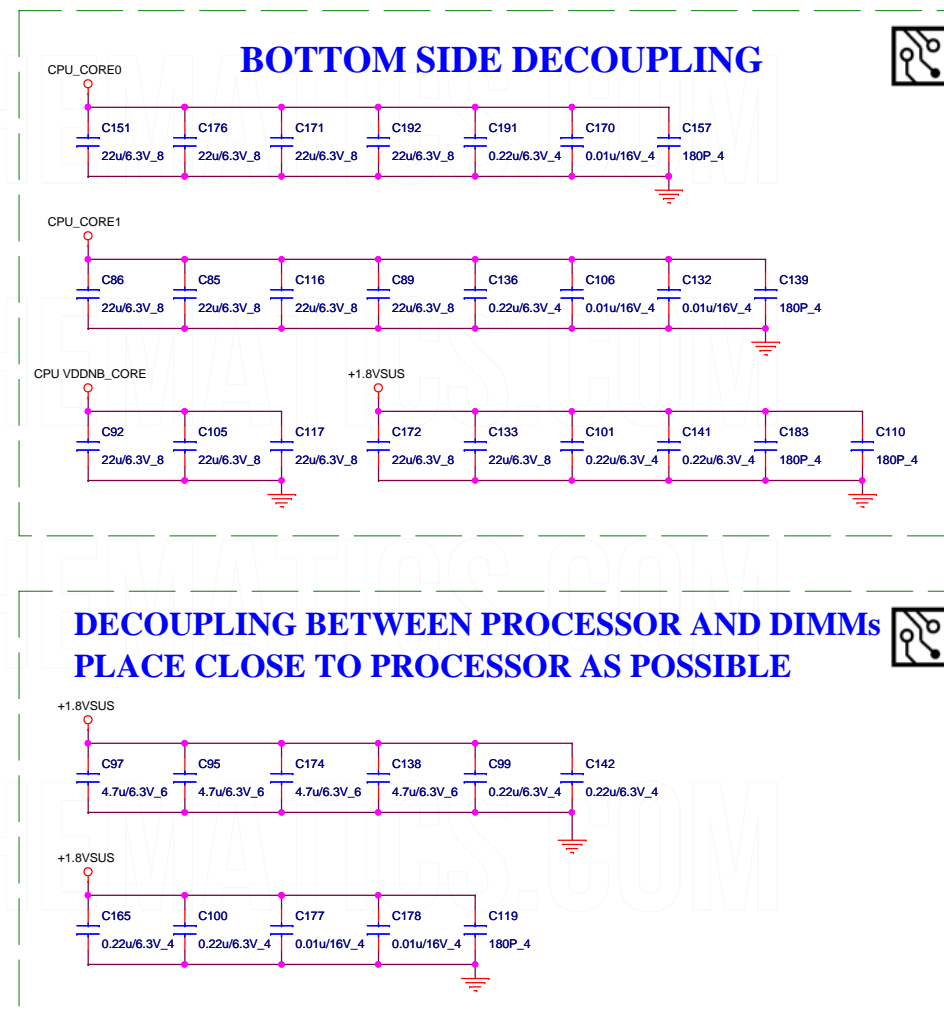


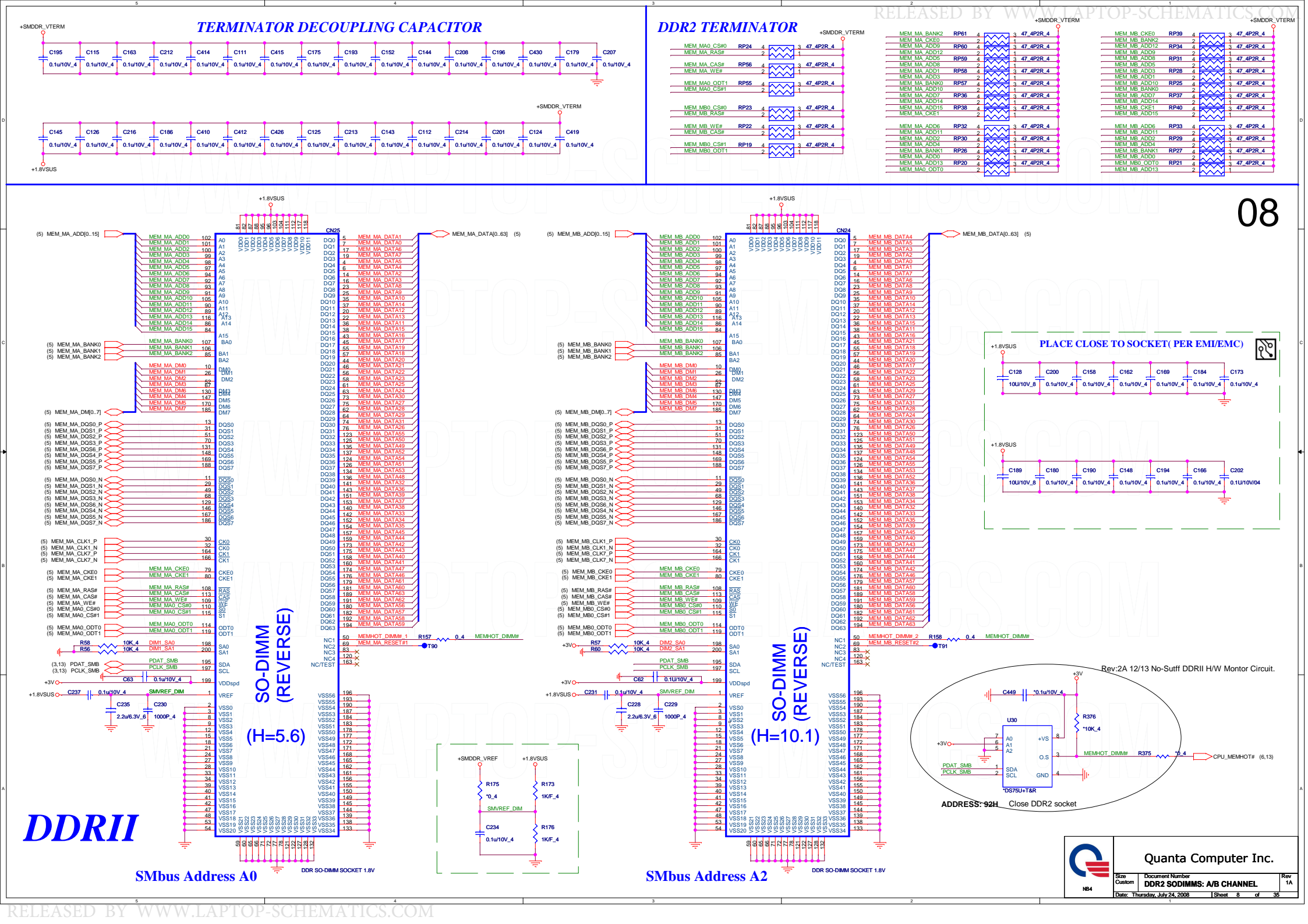
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 CTRL & DEBUG 3/4	1A
Date: Thursday, July 24, 2008	Sheet 6 of 35	

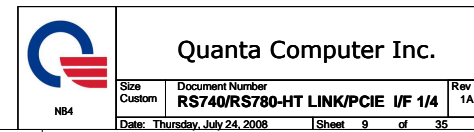


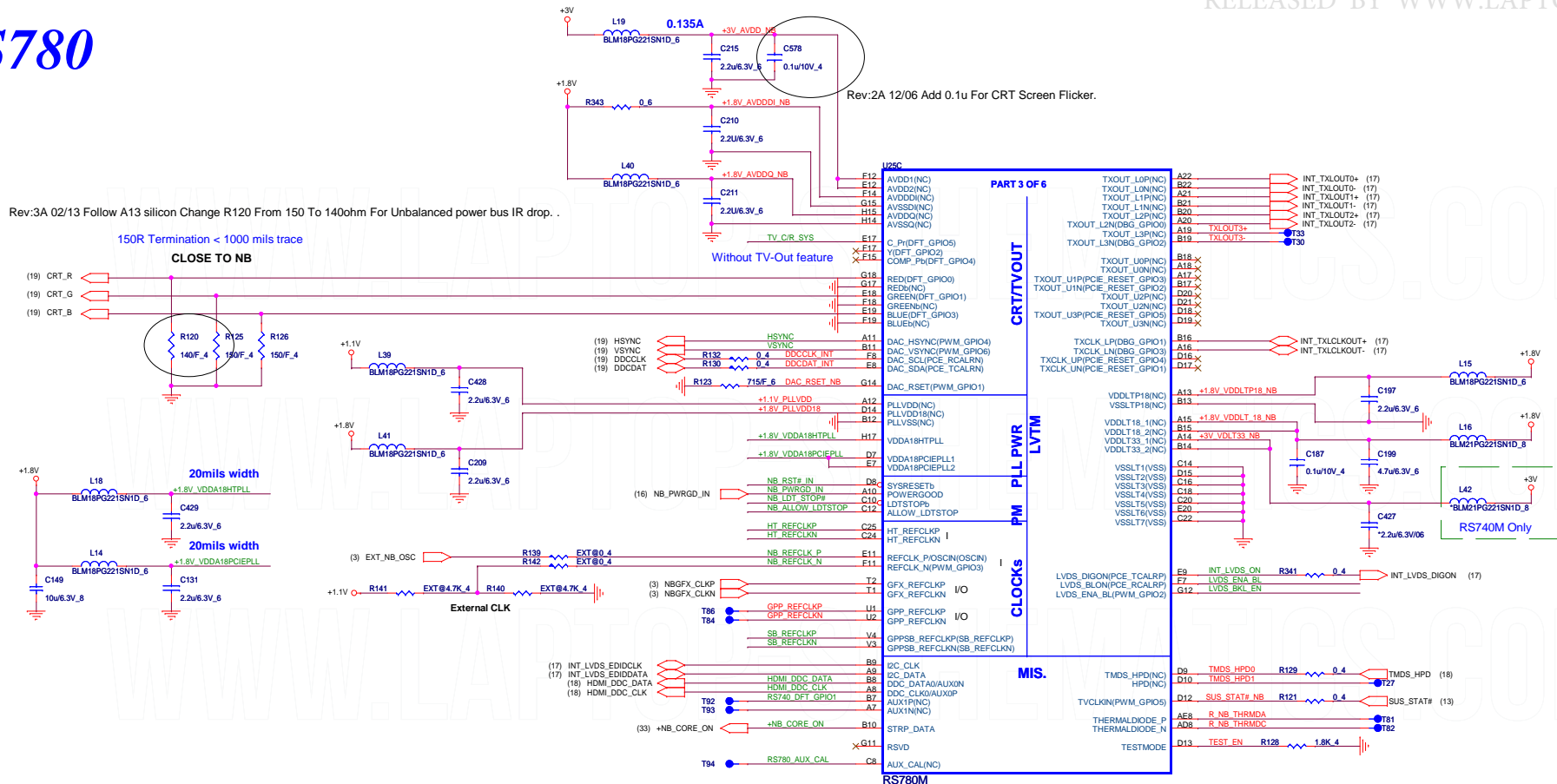
PROCESSOR POWER AND GROUND



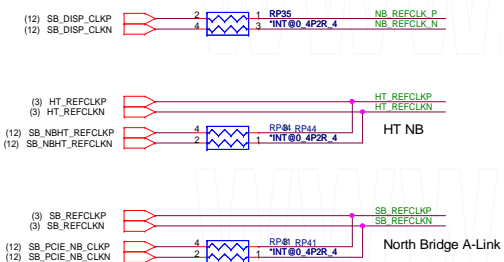


DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1





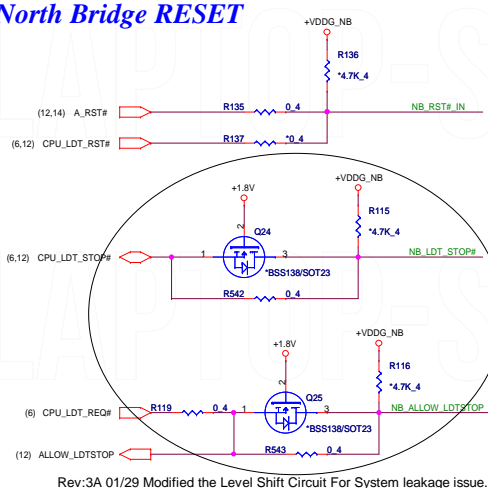
FOR SB INTERNAL CLOCK



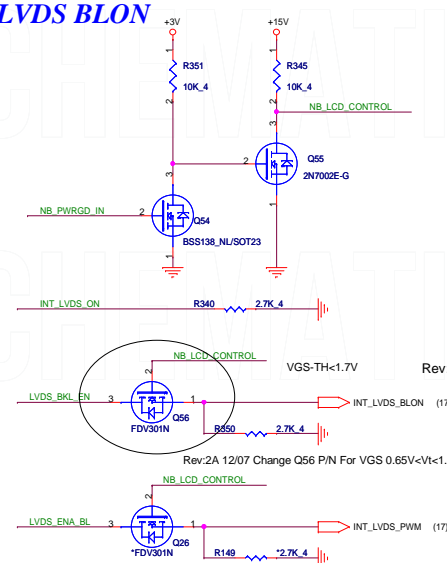
Reserve Pin



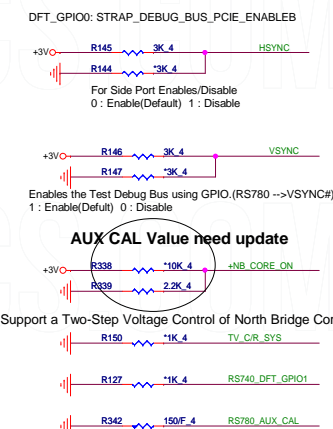
North Bridge RESET



LVDS BLON

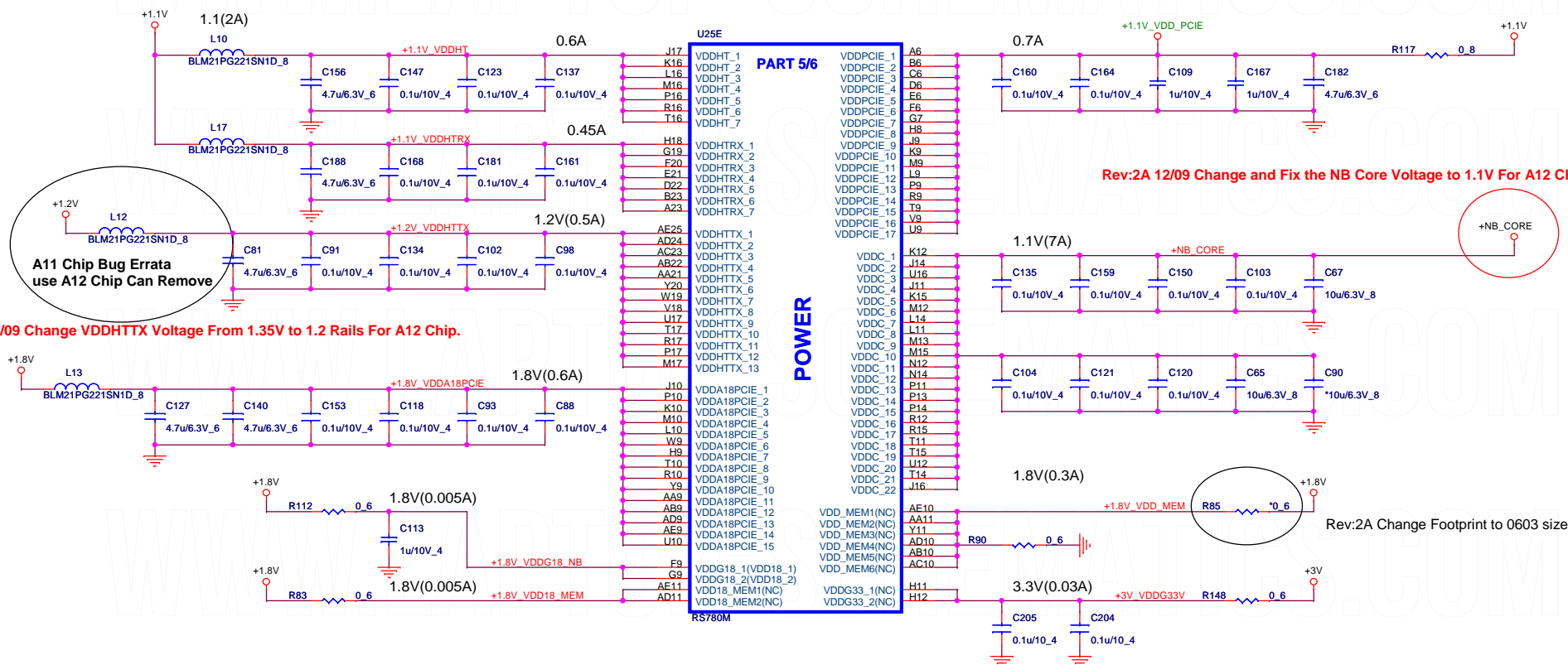


STRAP DEBUG BUS GPIO



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDO	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDLLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDLLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDLLT33	+3.3V	NC	NC



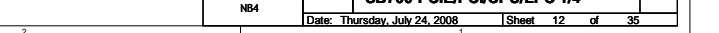
RS780

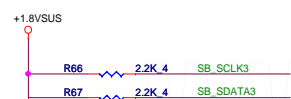


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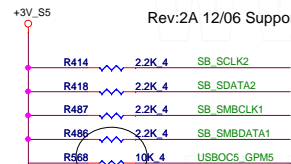
Size Custom	Document Number RS740/RS780-POWER5/5	Rev 1A
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FOR INTERNAL CLOCK

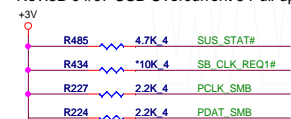




Rev:2A 12/06 Support the New Card Hot Plug Function.

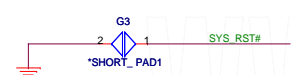


Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.



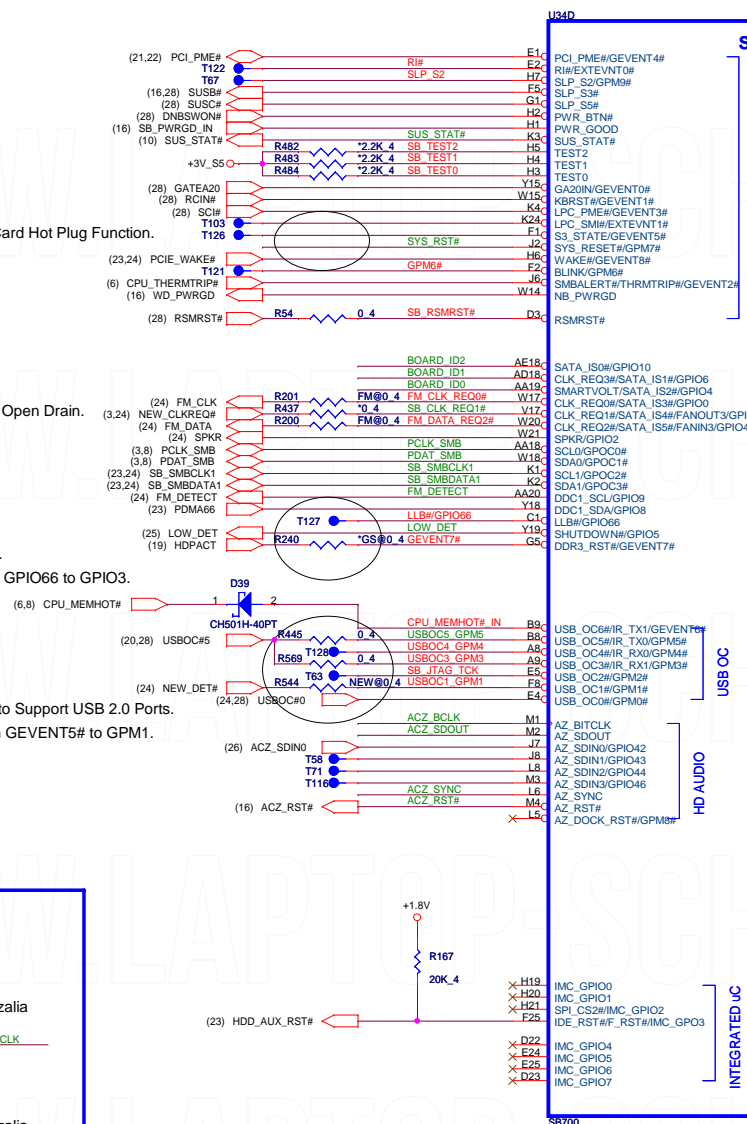
Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).

Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.



Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

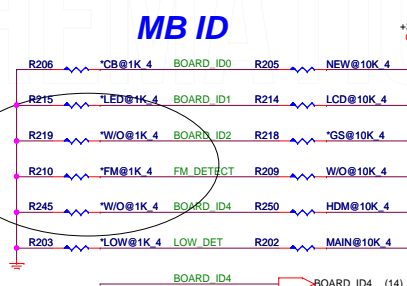
Rev:3A 02/05 Move Hot Plug Pin Name From GEVENT5# to GPM1.



MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H L					
W/ CCFL Panel W/ LED Panel		H L				
W/ G-Sensor W/O G-Sensor			H L			
W/O FM W/FM				H L		
W/ HDMI W/O HDMI					H L	
Main Strom Low Cost						H L

MB ID

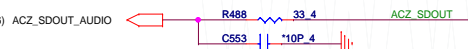


HD Audio Interface

To Azalia



To Azalia



To Azalia



To Azalia



Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K



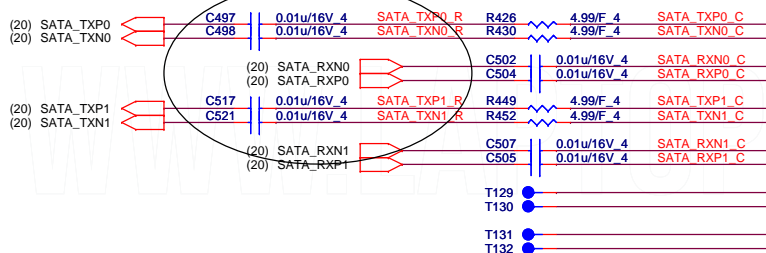
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Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Re 1
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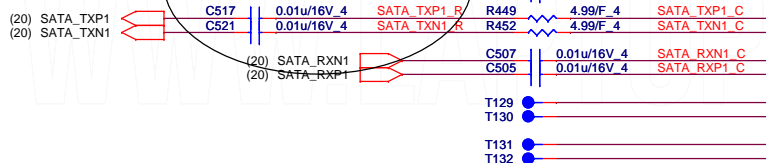
SB700

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

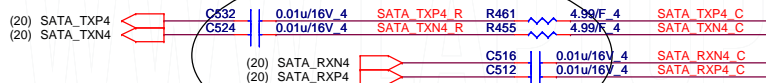
SATA HDD



E-SATA

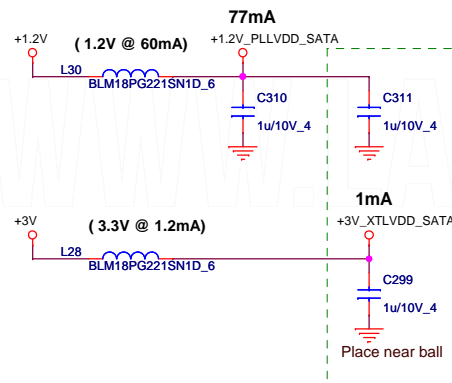
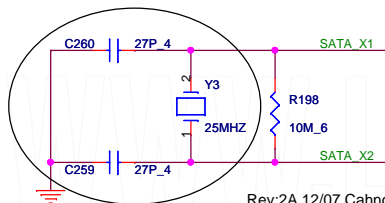


SATA ODD



NOTE:

R635 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



U34B

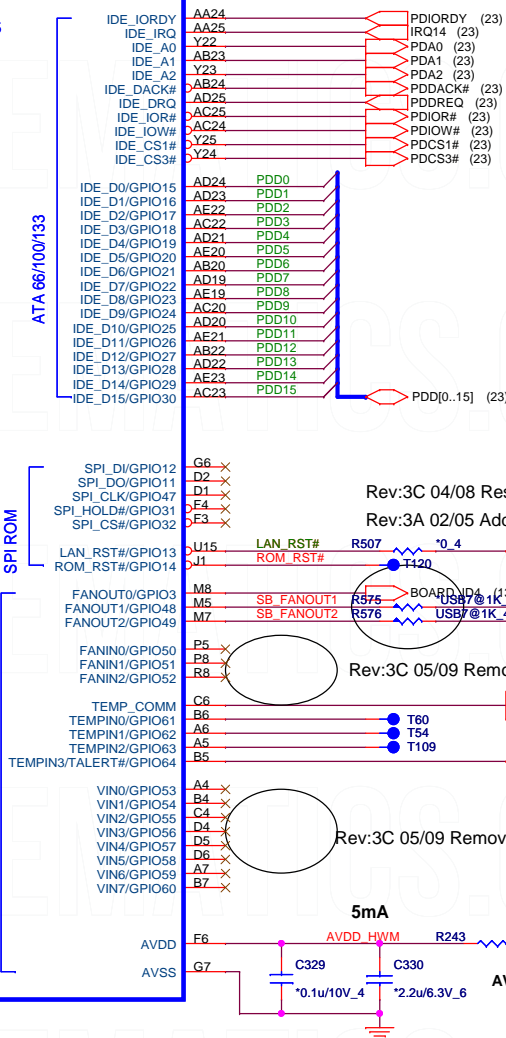
SB700

Part 2 of 5

SERIAL ATA

SATA PWR

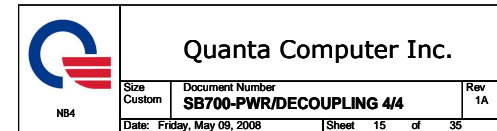
HW MONITOR

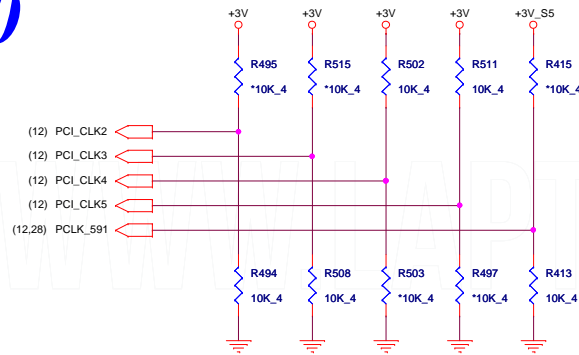


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Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A
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~~A11 Chip Bug~~ use A12 Chip Can Remove

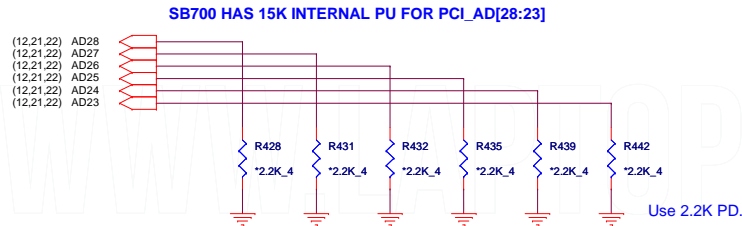




REQUIRED STRAPS

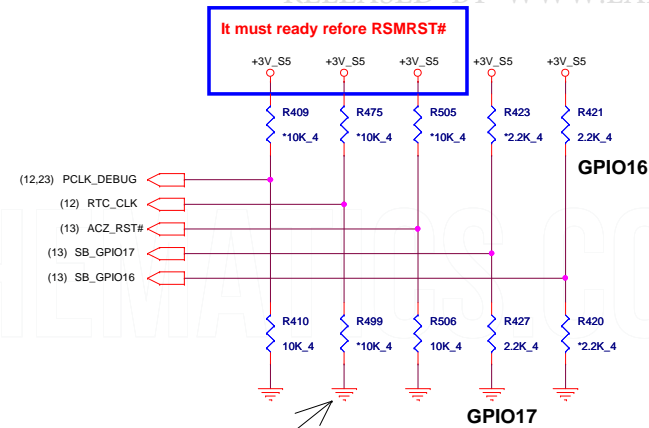
PULL HIGH	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED <small>DEFAULT</small>	IGNORE DEBUG STRAPS <small>DEFAULT</small>			DISABLE PCI MEM BOOT <small>DEFAULT</small>

DEBUG STRAPS



REQUIRED STRAPS

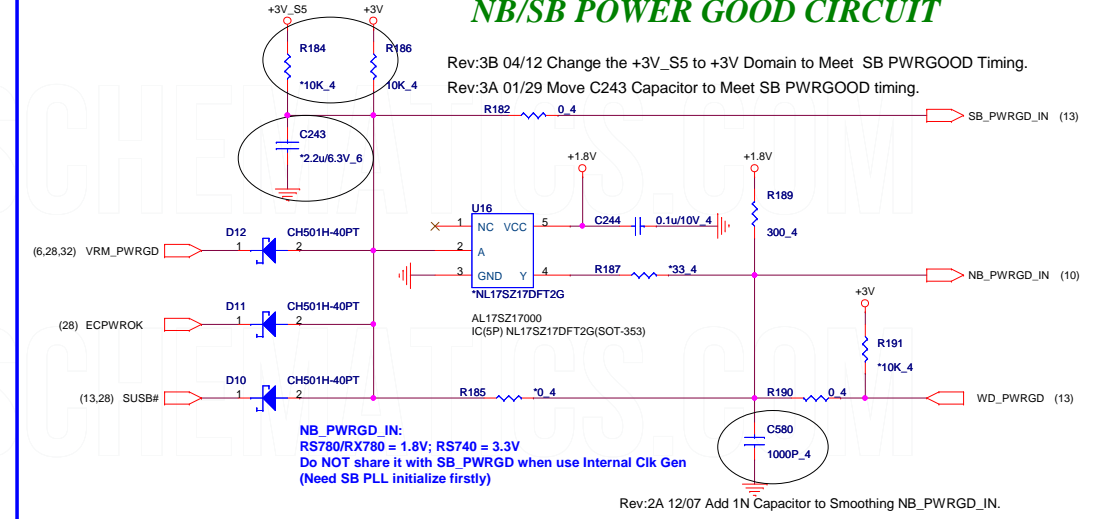
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET <small>DEFAULT</small>	USE PCI PLL <small>DEFAULT</small>	USE ACPI BCLK <small>DEFAULT</small>	USE IDE PLL <small>DEFAULT</small>	USE DEFAULT PCIE STRAPS <small>DEFAULT</small>	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

PULL HIGH	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
	CLKGEN ENABLED	INTERNAL RTC <small>DEFAULT</small>	EC ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	CLKGEN DISABLED <small>DEFAULT</small>	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED <small>DEFAULT</small>		L, H = LPC ROM <small>DEFAULT</small> L, L = FW ROM

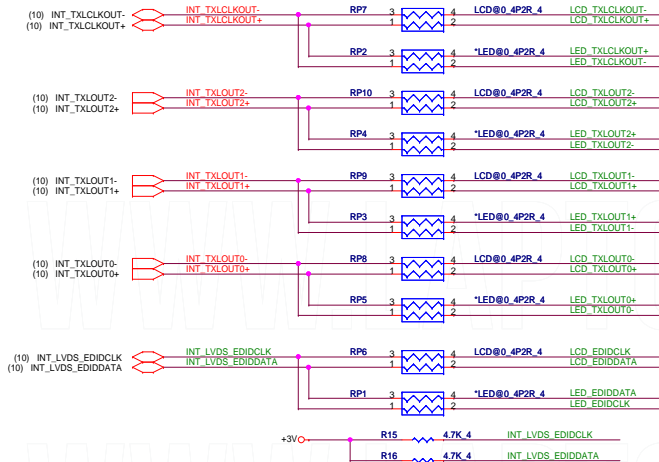
NB/SB POWER GOOD CIRCUIT



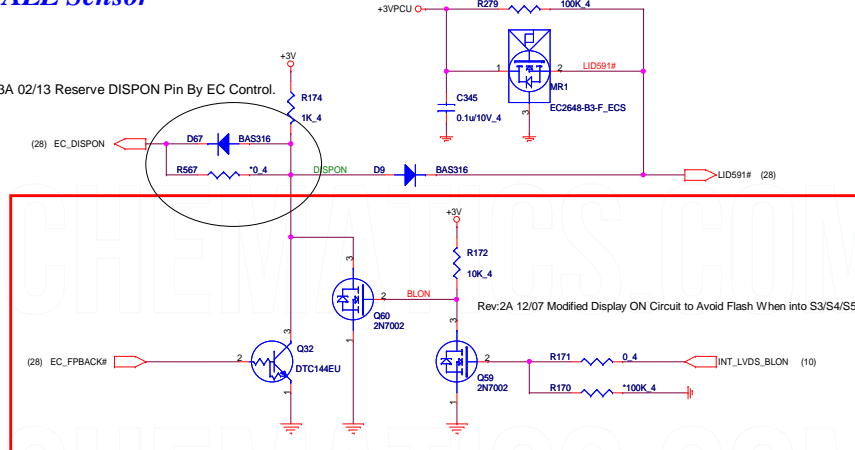
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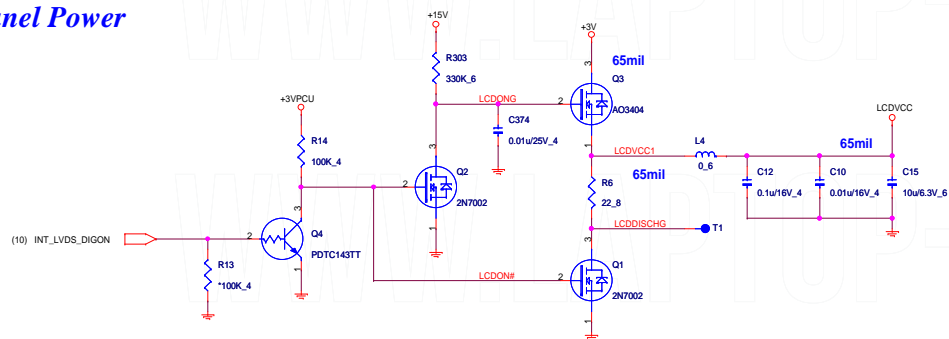
HALL Sensor



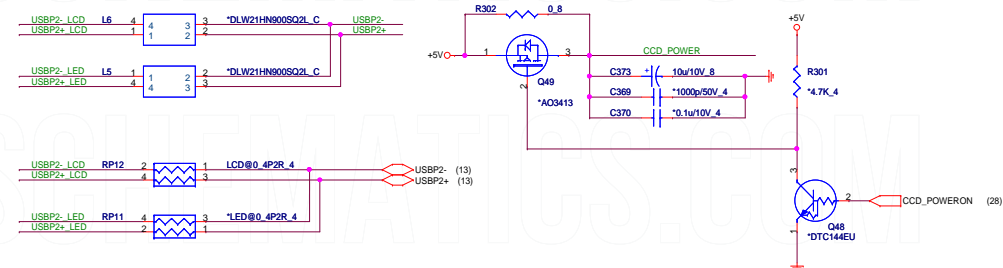
Rev:3A 02/13 Reserve DISPON Pin By EC Control



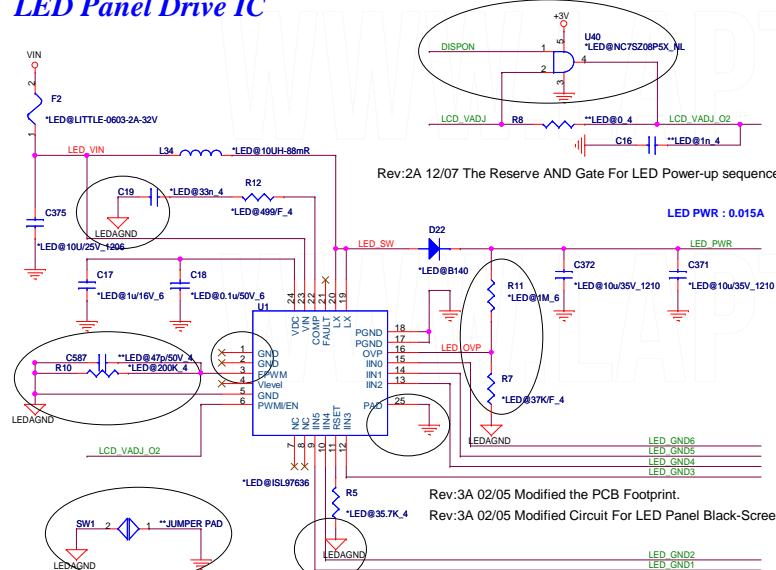
Panel Power



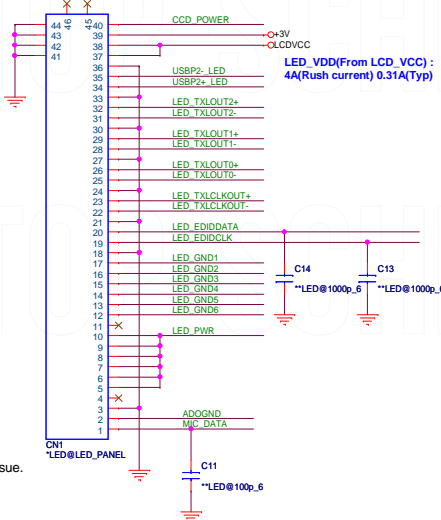
CAMERA Module



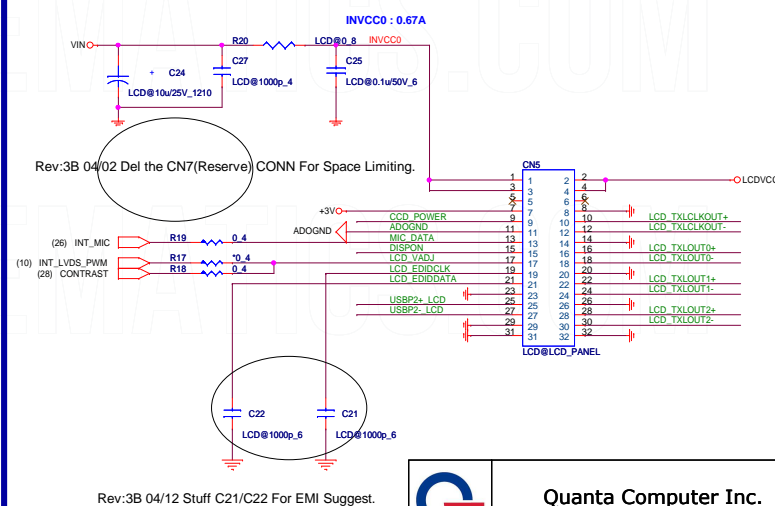
LED Panel Drive IC



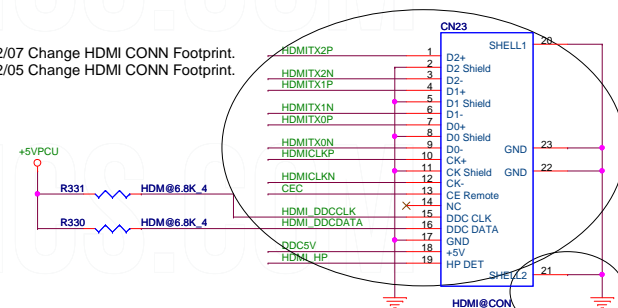
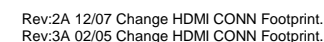
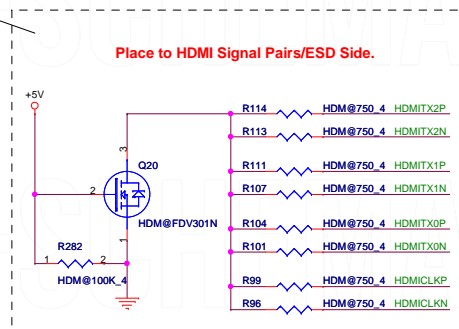
TOSHIBA LED Panel Module



LCD Panel Module

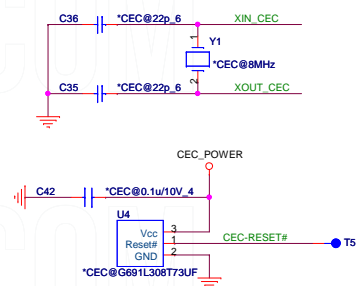
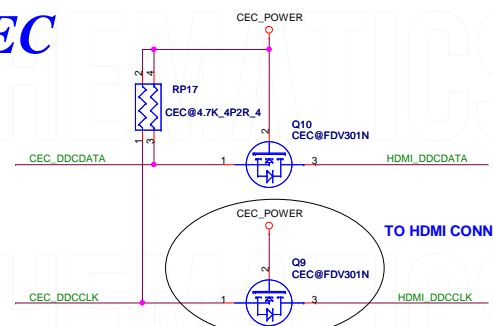


Place to HDMI Signal Pairs/ESD Side.



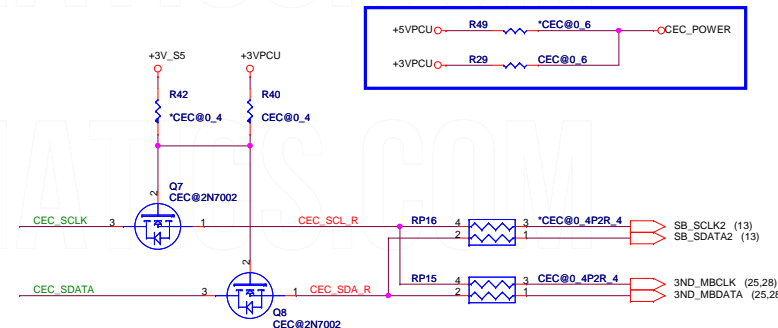
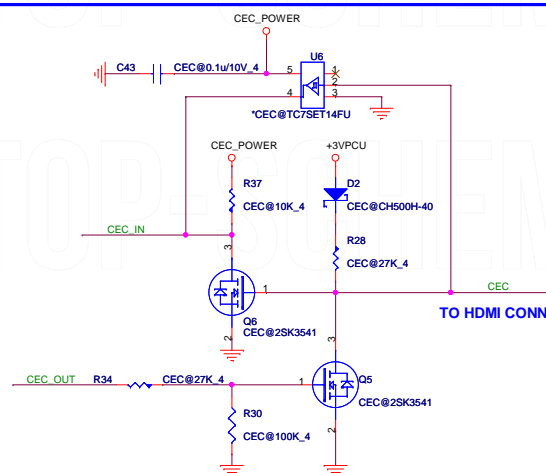
Rev:3A 02/05 Change PIN20/21/22/23 To Ground For ESD. EMI GROUND

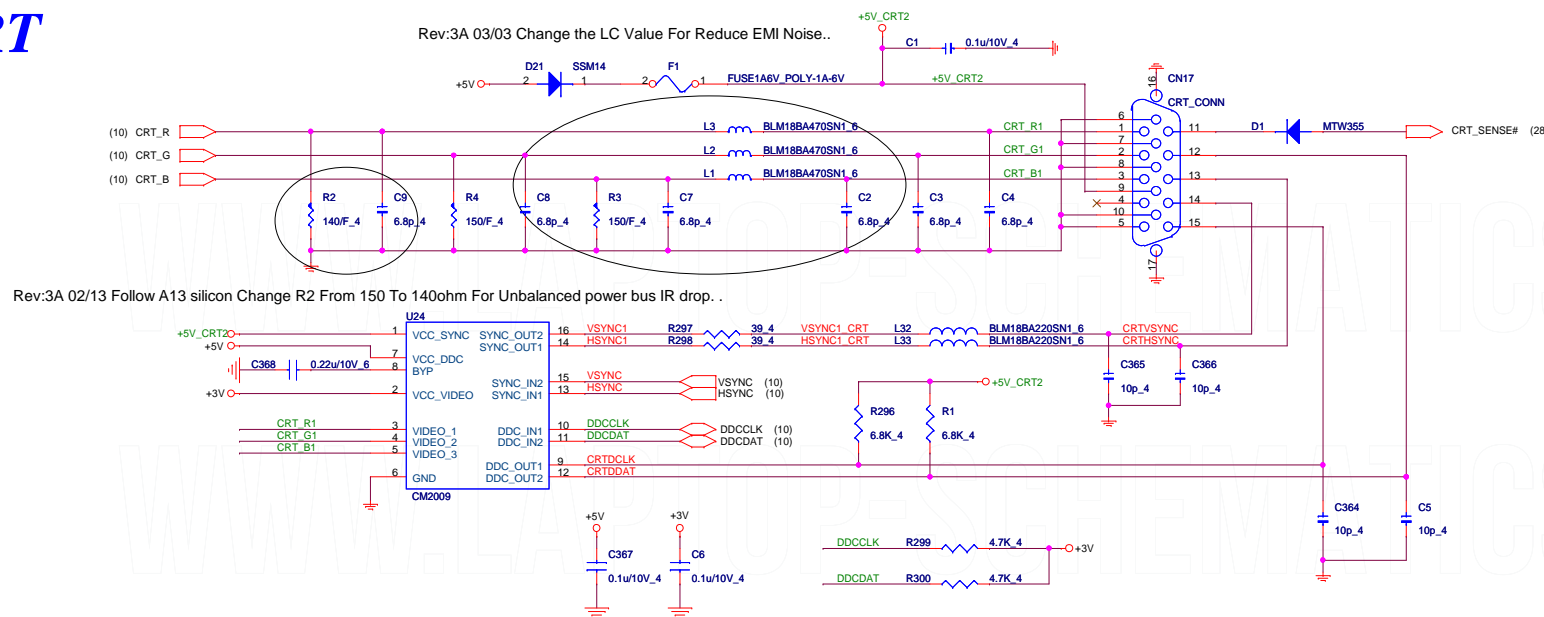
Clock/Test Pad



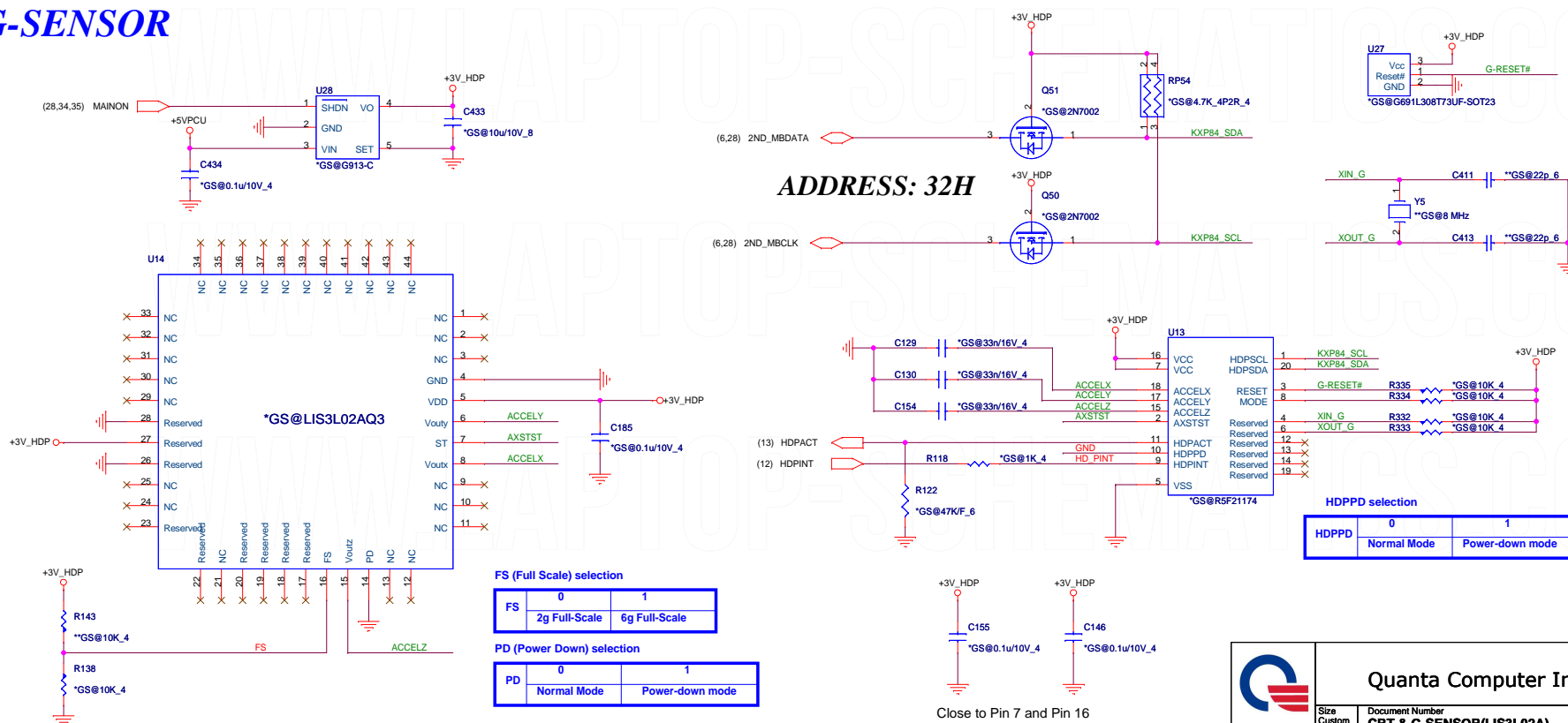
Rev:3A 03/03 Change the CECC V1.10 (P/N R5F211A4C22SP)

Rev:2A 12/07 Level Shift Circuit Wrong Change to Pull-up CEE POWER Domain.





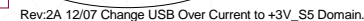
G-SENSOR



Close to Pin 7 and Pin 16



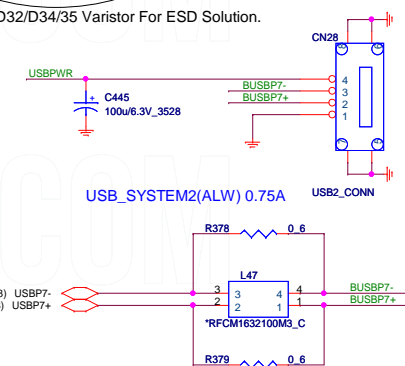
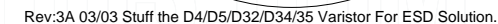
Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode...

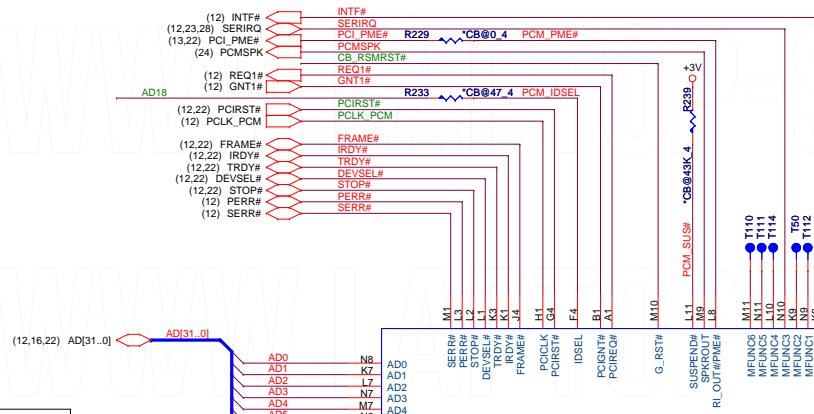
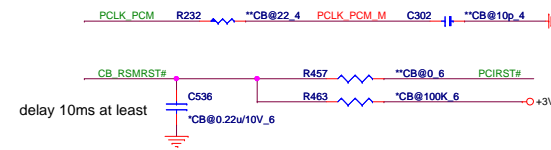
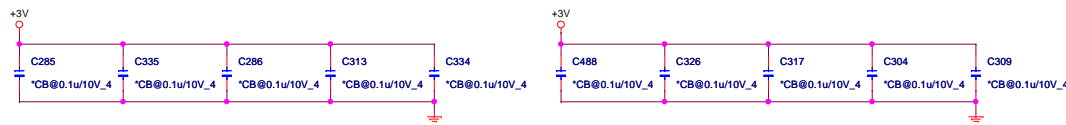


Rev:3A 01/29 Added Varistor ESD Solution

~~Rev:3A 02/13 Added the Re-Driver IC For ESATA.~~

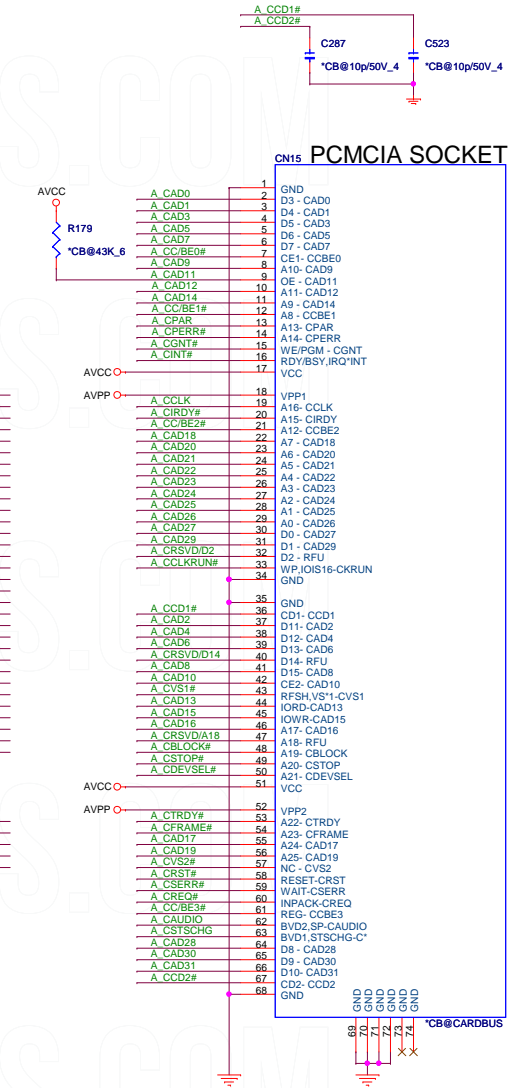
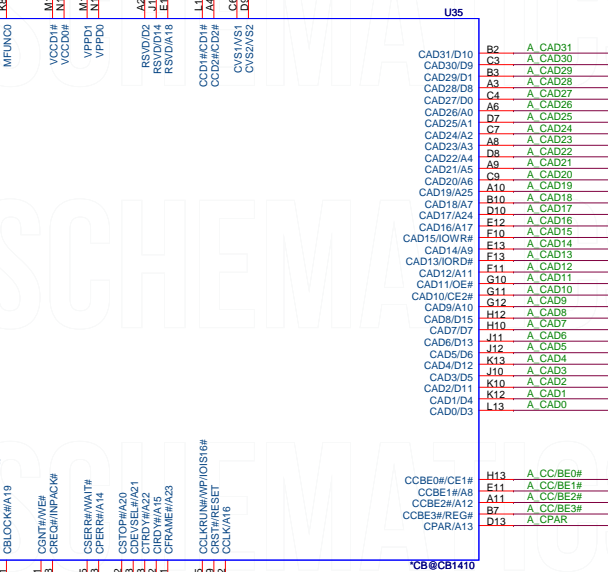
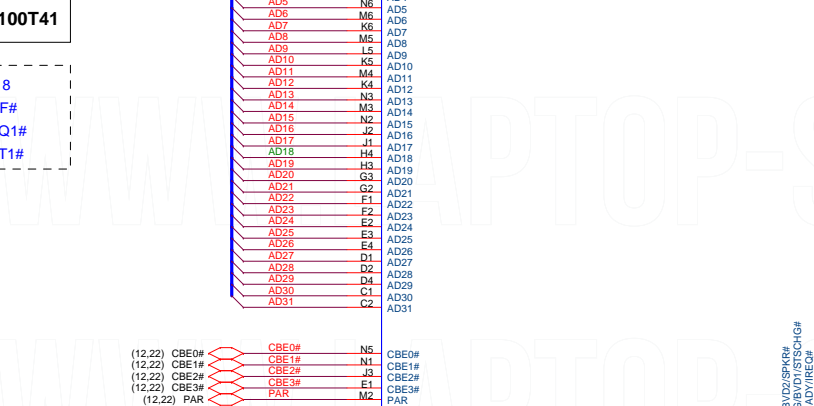
SEL0_X	SEL1_X	E _q	SEL2_X	Swing		SEL3_X	De-Emphasis
0	0	0dB	0	1.0X		0	0dB
0	1	2.5dB	1	1.2X		1	-3.5dB
1	0	4.5dB					
1	1	6.5dB					





ENE1410 AJ014100T41

ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ1#
Grant Indicate : GNT1#



CARDBUS

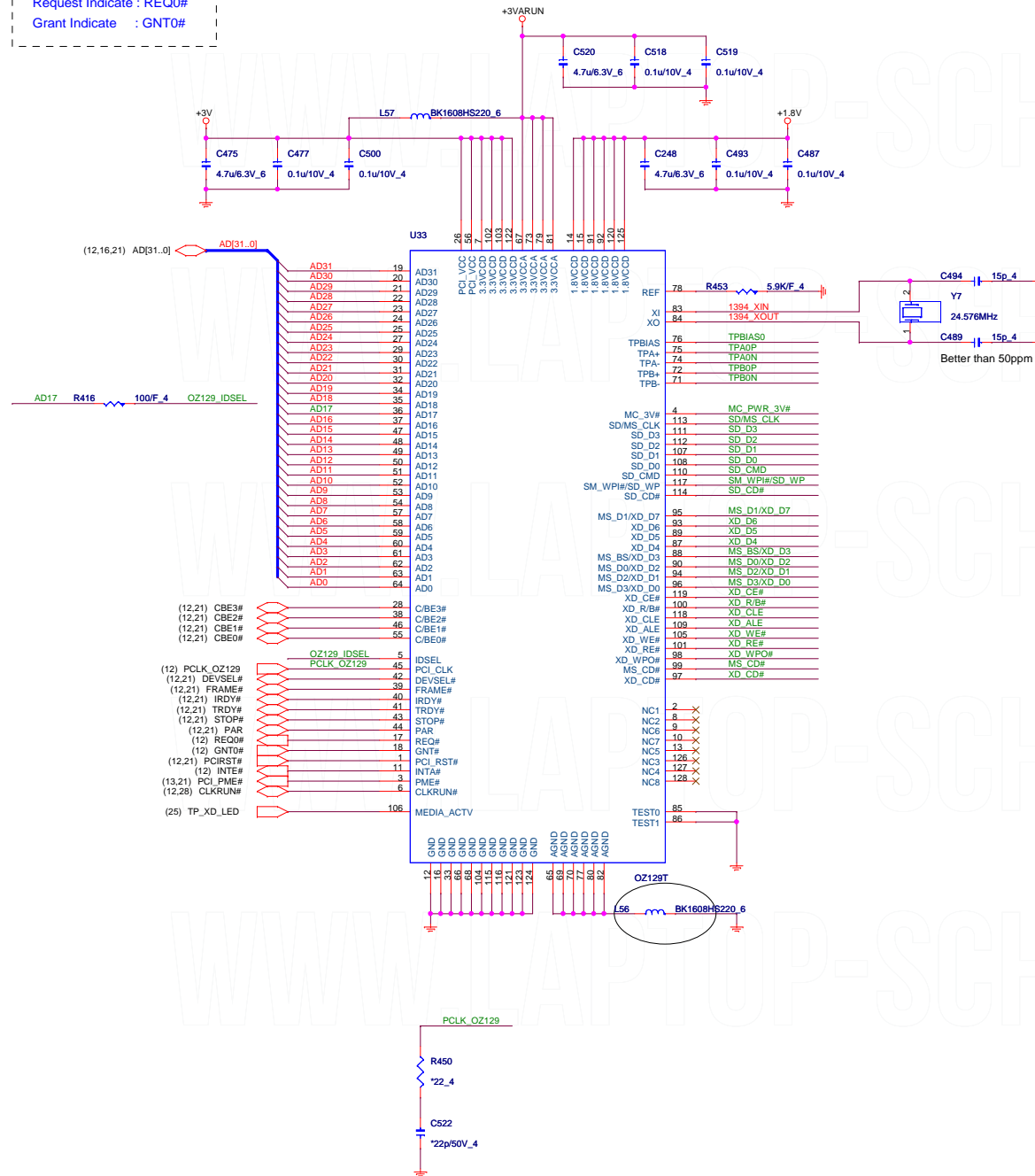
Quanta Computer Inc.

Size Custom Document Number PCMCIA(CB1410)-OPTION Rev 1A

Date: Thursday, July 24, 2008 Sheet 21 of 35

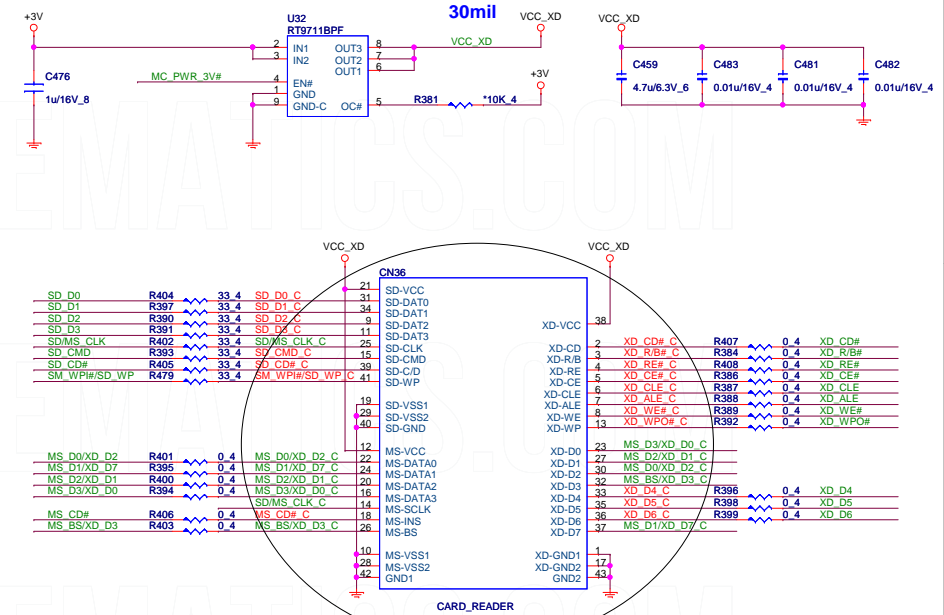
OZ129 CardReader/1394

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ0#
Grant Indicate : GNT0#

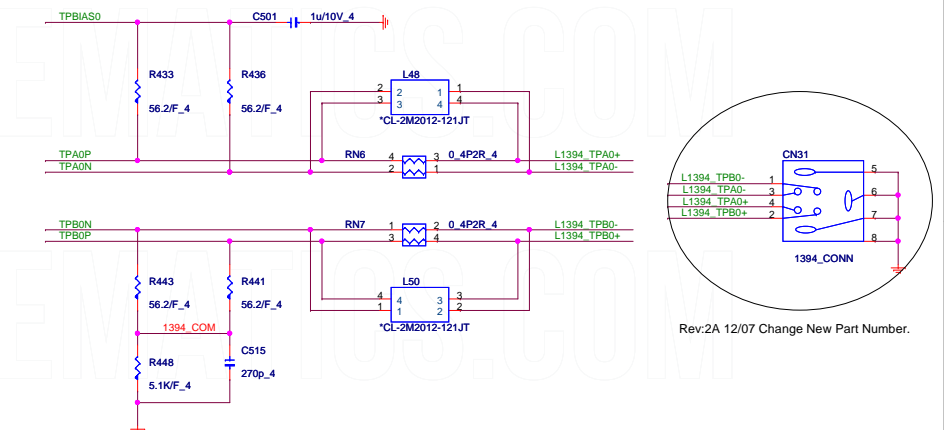


5 IN 1 Card Reader

22



1394

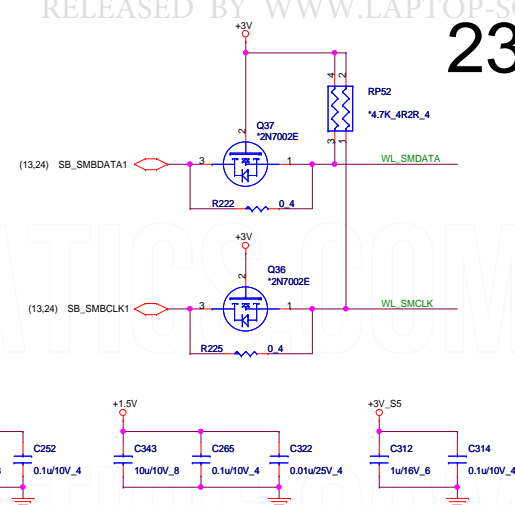
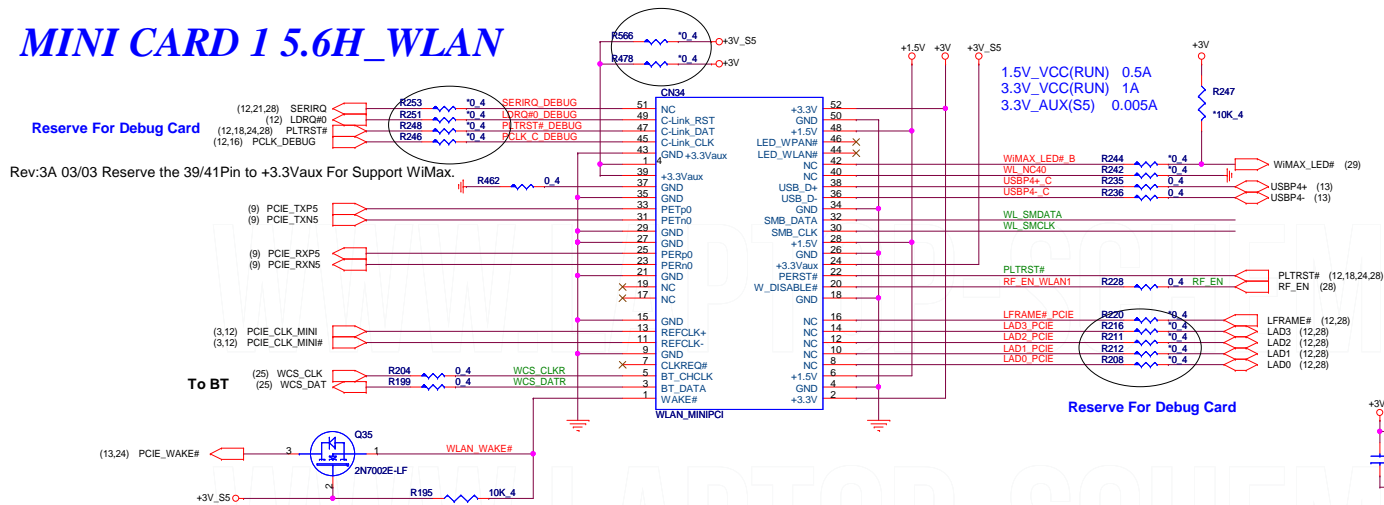


Quanta Computer Inc.

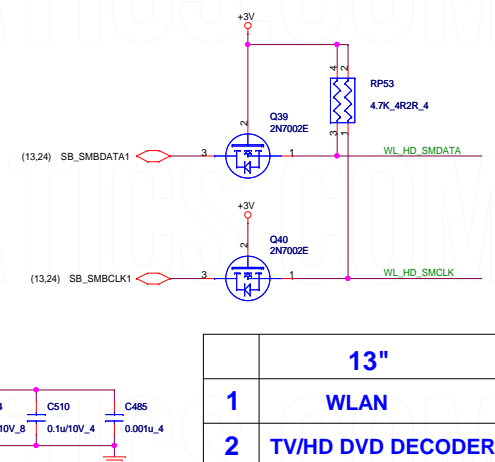
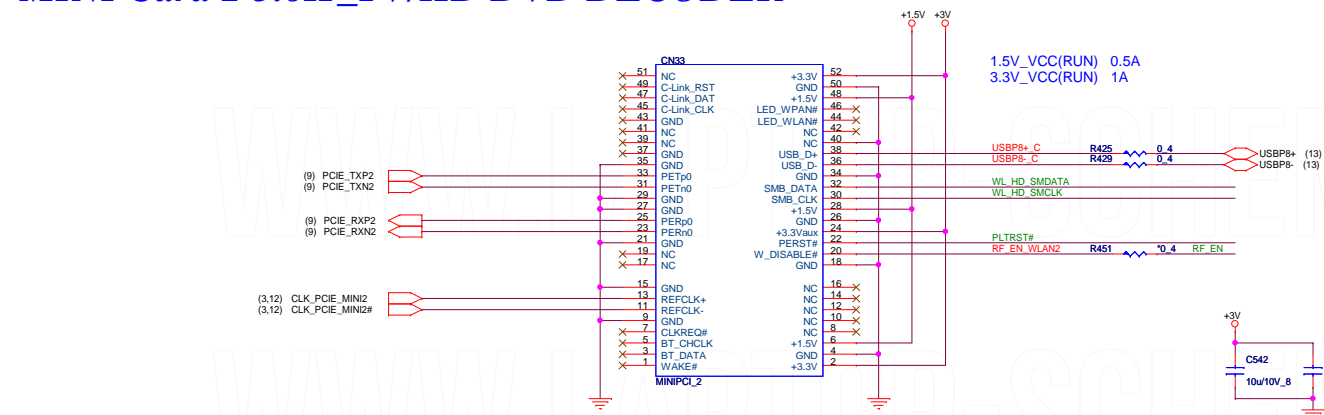
Size: Custom
Document Number: OZ129T(SIN1/1394)
Date: Thursday, July 24, 2008
Sheet: 22 of 35
Rev: 1A

MINI CARD 1 5.6H_WLAN

23

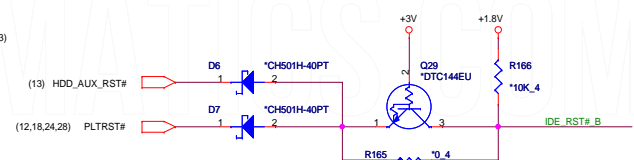
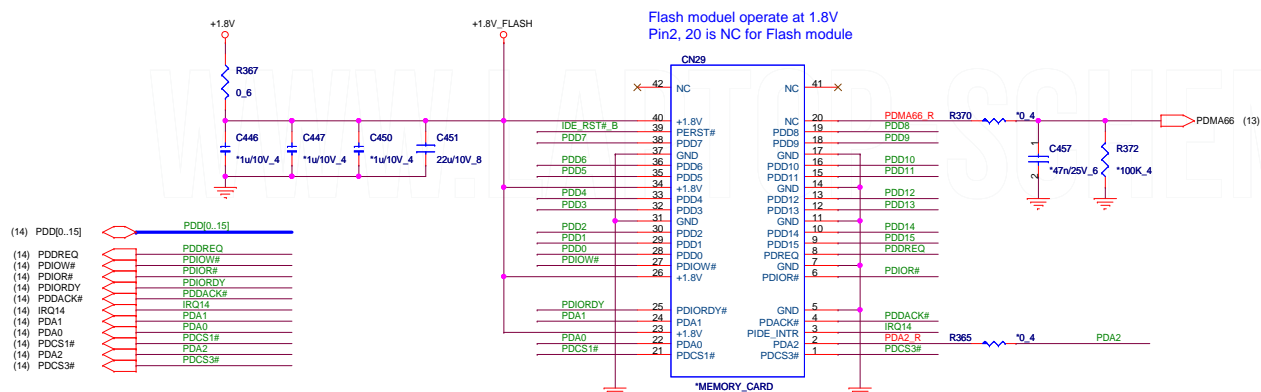


MINI Card 2 5.6H_TV/HD DVD DECODER

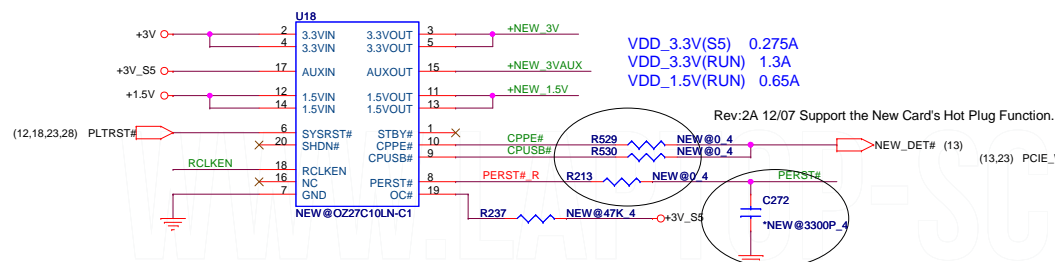


	13"
1	WLAN
2	TV/HD DVD DECODER

NAND FLASH MEMORY CARD

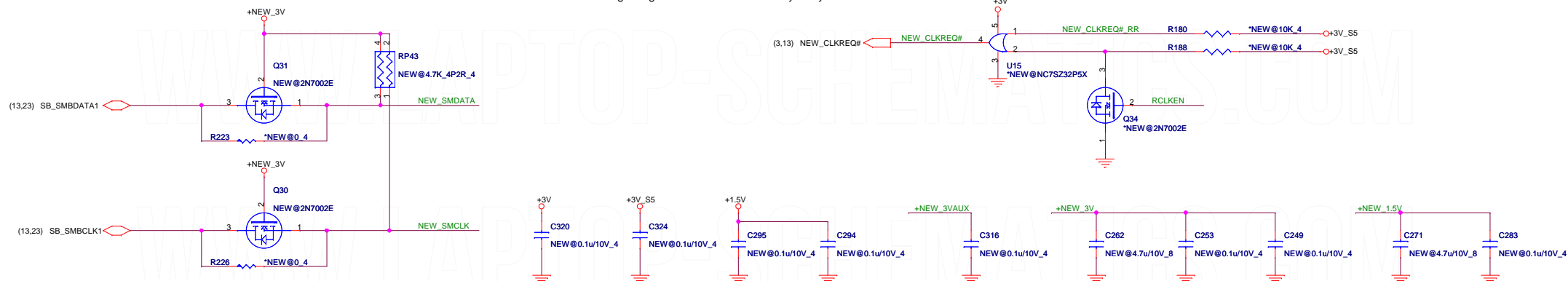


NEW CARD(BTO)

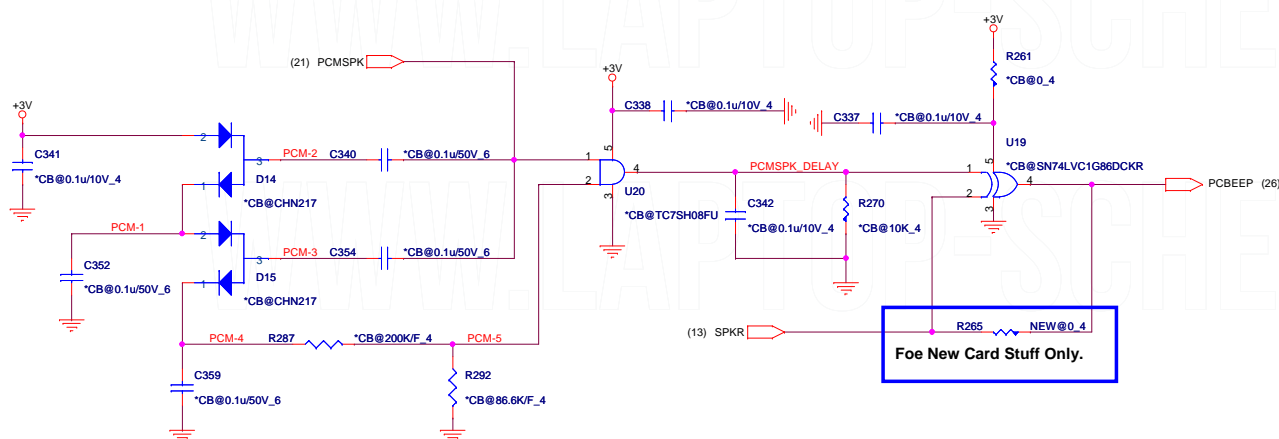


NEW CARD'S POWER SWITCH

Rev:3A 03/03 As check with AE regarding to PERST# do not add any delay into PERST#

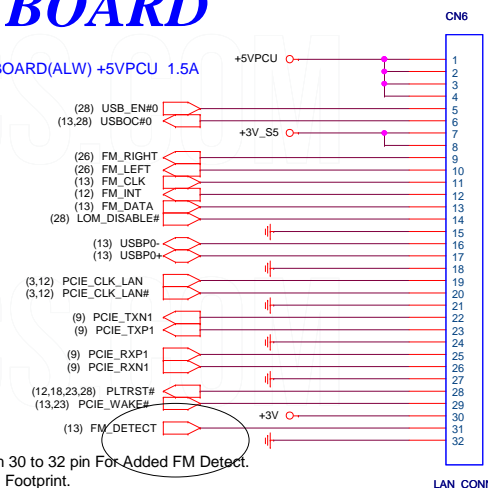


PC-BEEP



RJ45/USB BOARD

USB & LAN BOARD(ALW) +5VPCU 1.5A



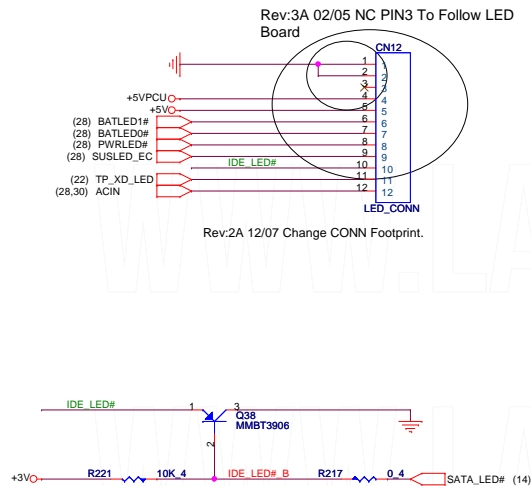
Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.
Rev:3A 02/05 Change Connector PCB Footprint.



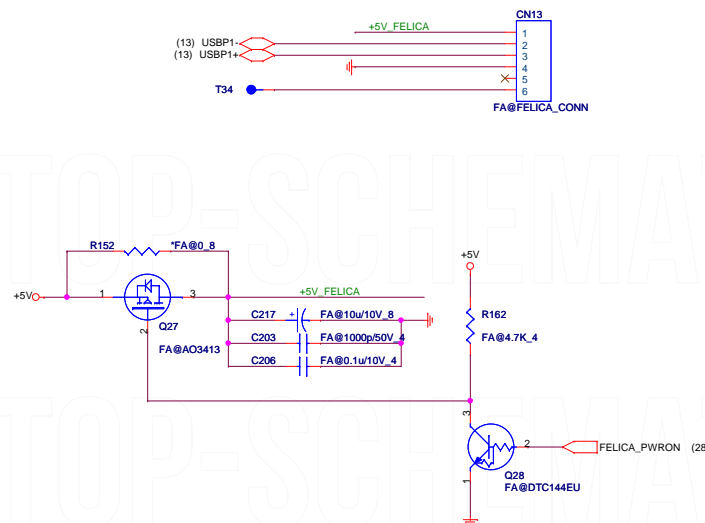
Quanta Computer Inc.

Size Custom	Document Number NEW CARD & RJ45 BOARD/BEEP	Rev 1A
Date: Thursday, July 24, 2008		Sheet 24 of 35

LED BOARD

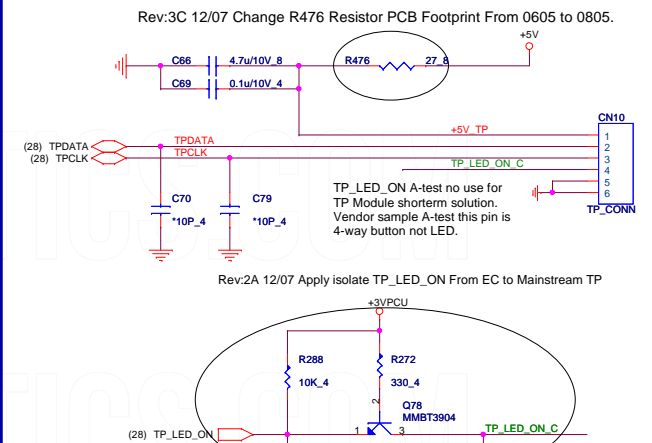


Felica

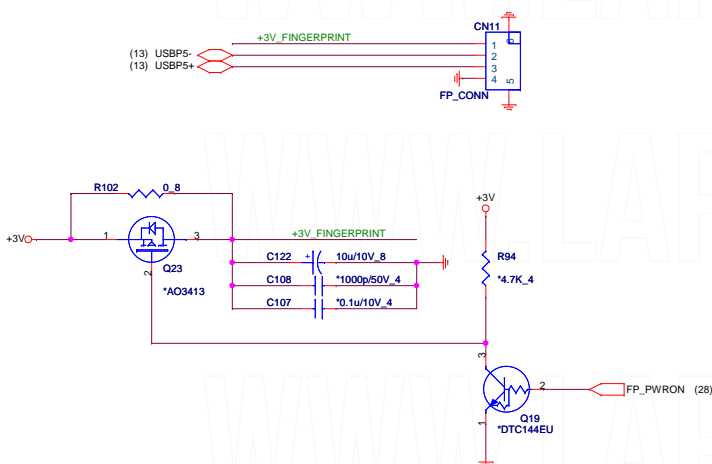


TP BOARD

25

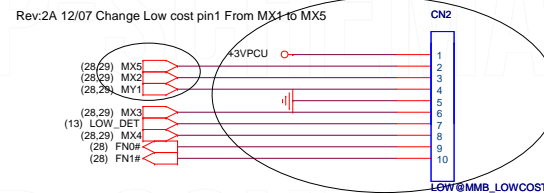


FINGER-PRINT



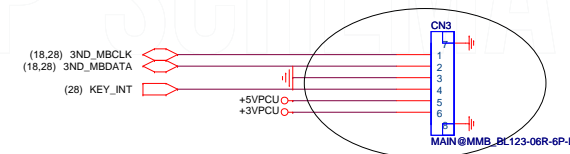
MMB

Low cost



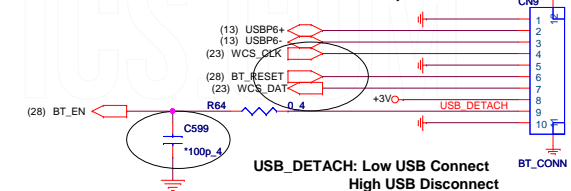
Rev:2A 12/07 Change CONN Footprint.

Main stream



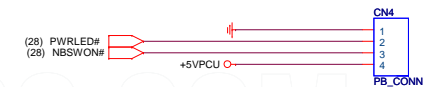
Bluetooth Module

Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77



Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

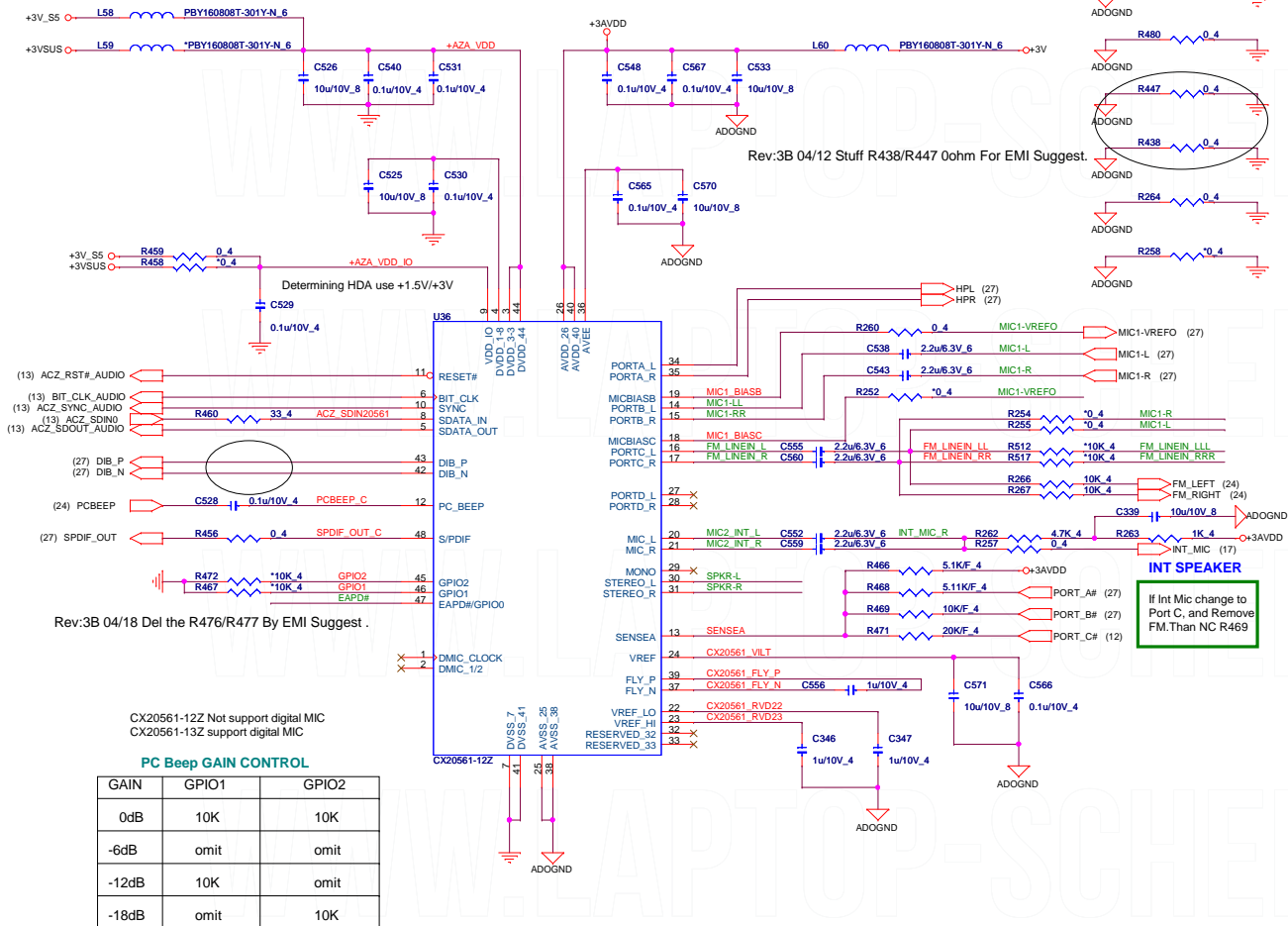
POWER BOARD



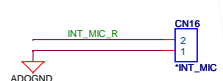
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/FP/BT/PB/FELICA/MMB CONN	1A
Date: Tuesday, August 19, 2008	Sheet 25 of 35	

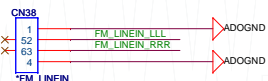
CODEC(CX20561)



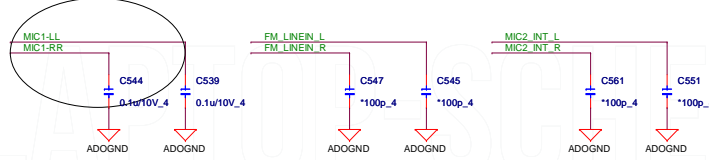
Reserve INTMIC



Reserve FM

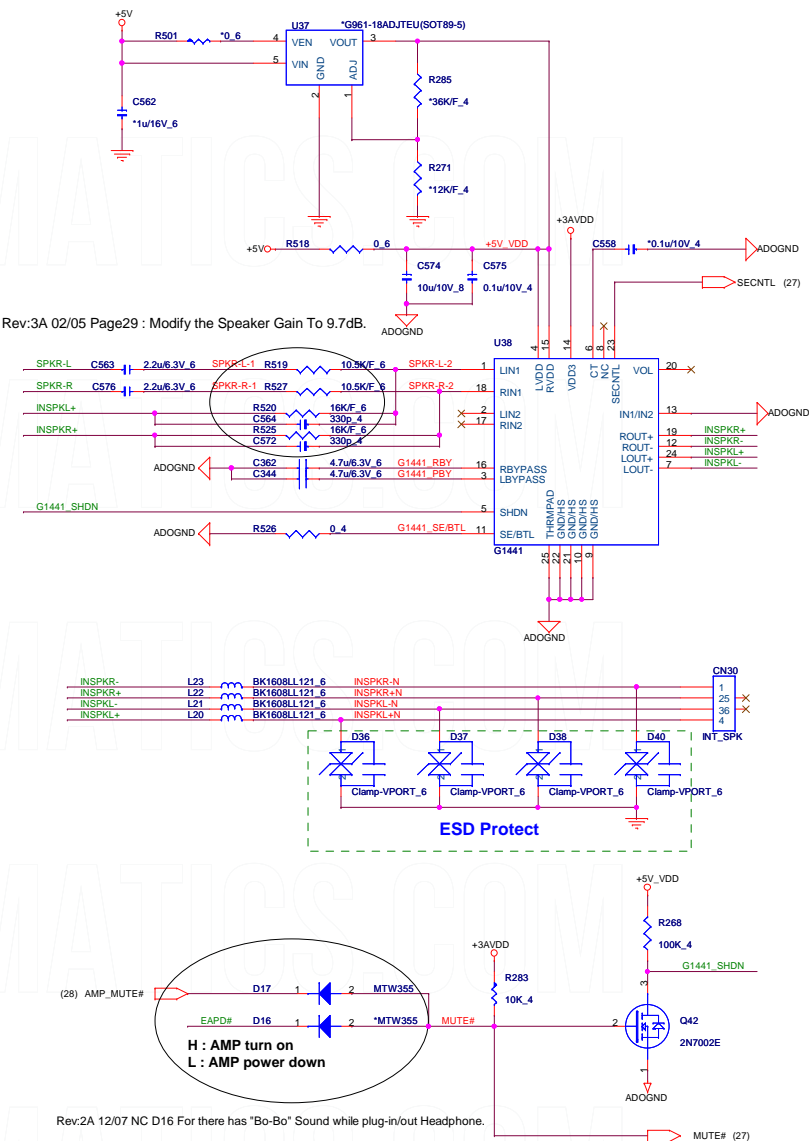


Rev:3A 02/05 Stuff C539/C544 For INT MIC Recording Noise.



INT SPK AMP

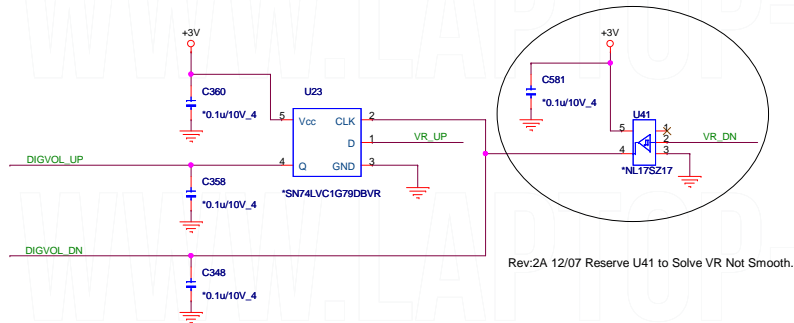
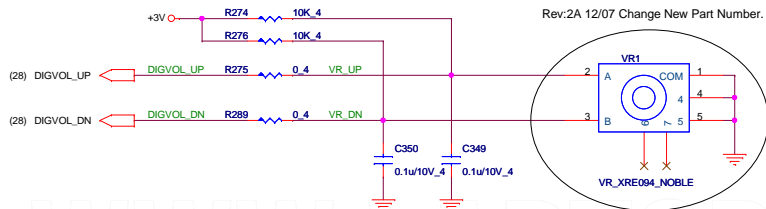
26



Quanta Computer Inc.

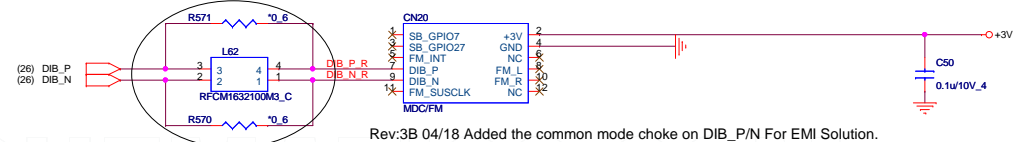
Size	Document Number	Rev
Custom	CONEXANT(CX205601)/SPK/AMP	1A
Date: Thursday, July 24, 2008	Sheet 26 of 35	

VR

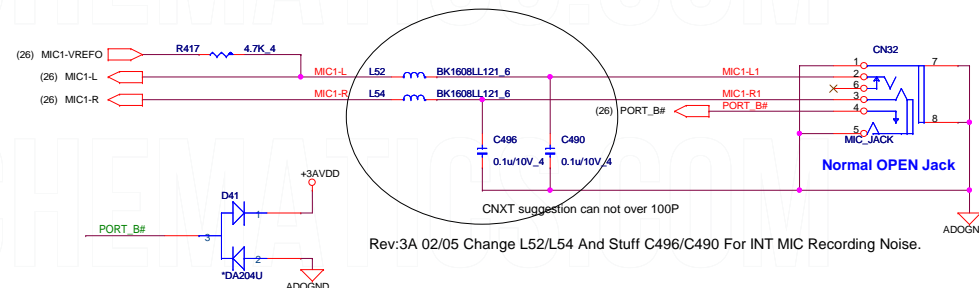


FM TUNER & MDC

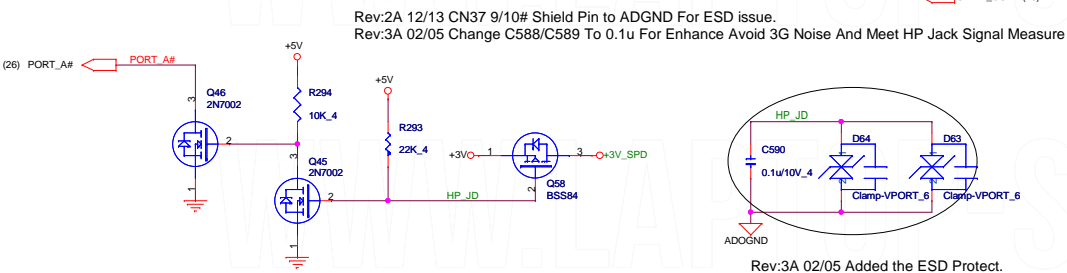
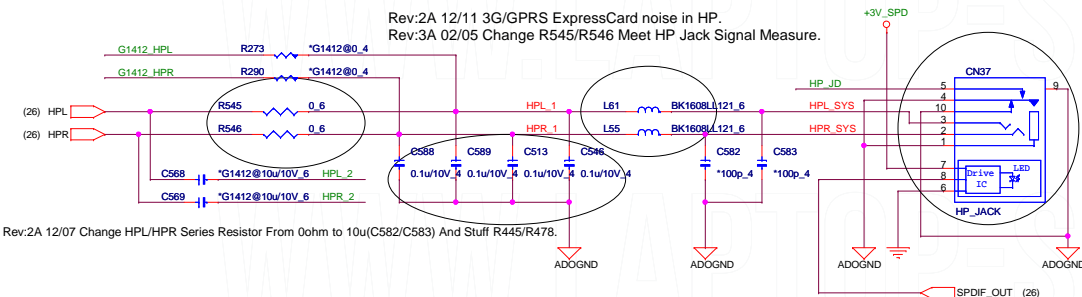
27



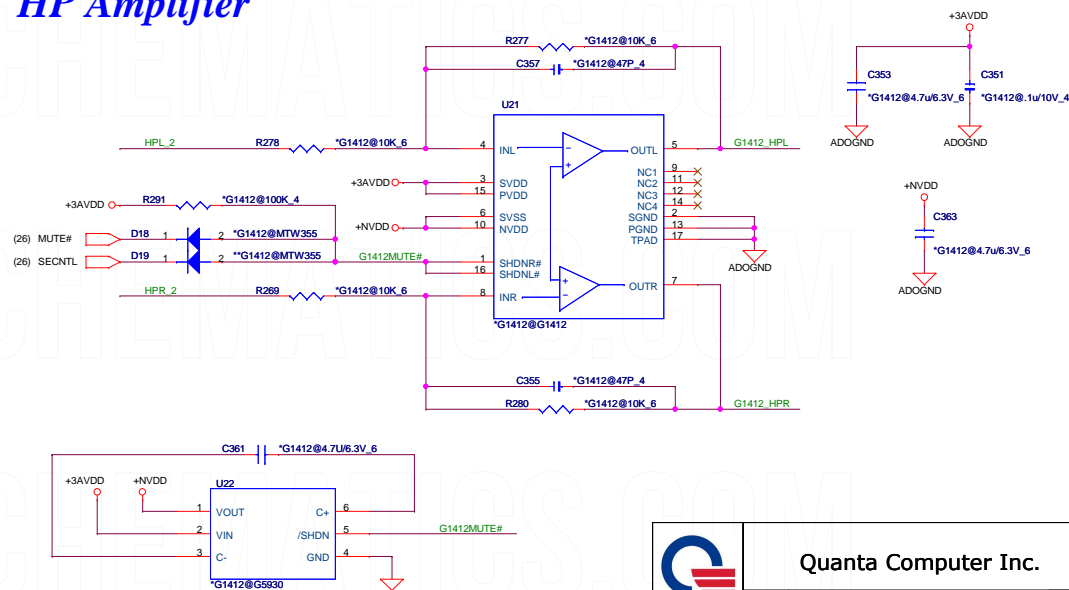
SYSTEM MIC



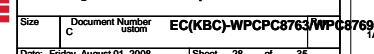
HP JACK



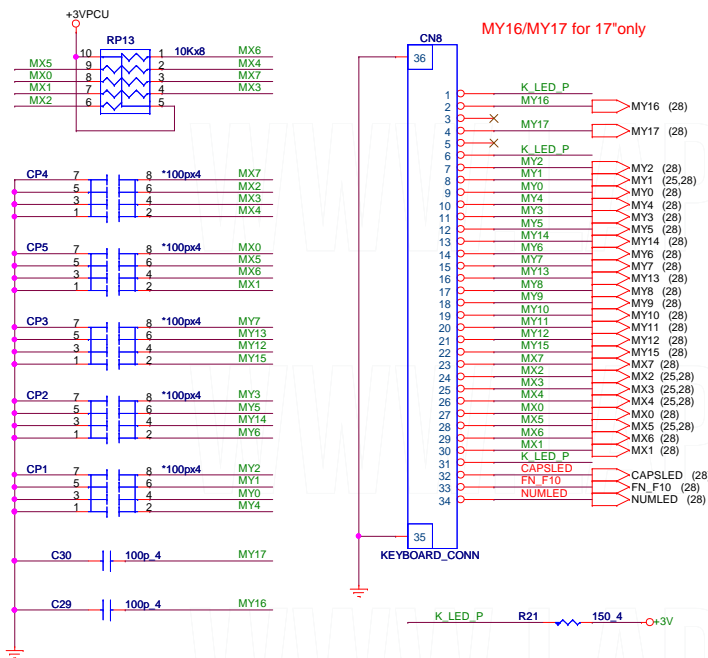
HP Amplifier



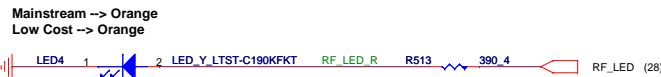
NB4	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	JACK/VR/FM/MIC/MDC/AMPLIFIER	1A
	Date:	Thursday, July 24, 2008	Sheet 27 of 35



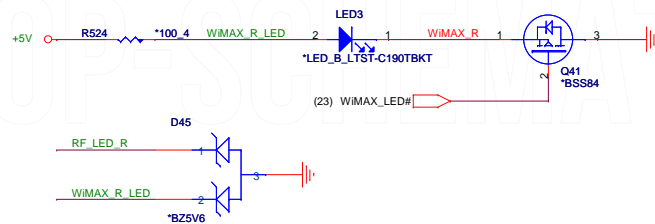
INT KEYBOARD



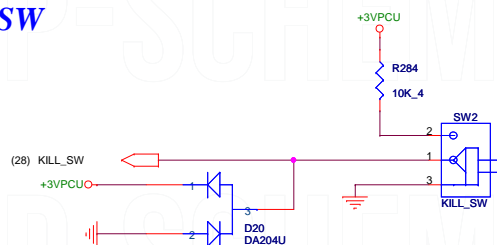
W-LAN&BT LED



WiMAX LED

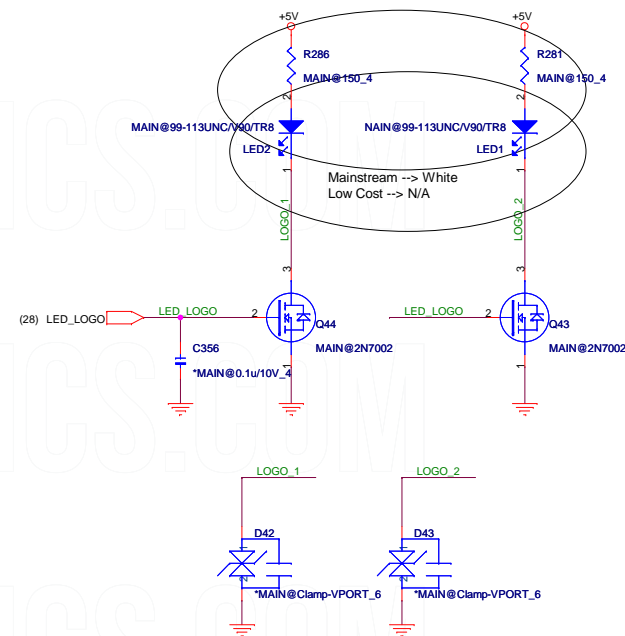


KILL SW



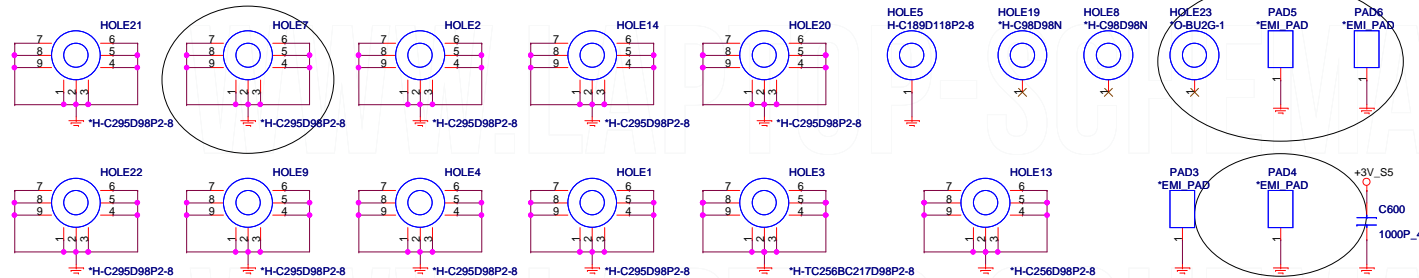
Satellite LED

Rev:2A 12/07 Updated the LED1/LED2 Footprint And Part Number.
Rev:3A 02/05 Change R281/R286 and R375 To 150ohm For LED Light Not Enough

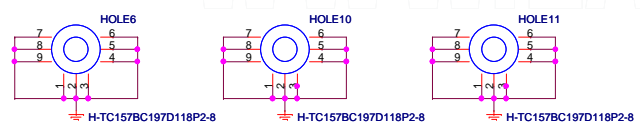


HOLE

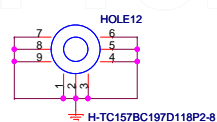
Rev:2A 12/09 Modified the Footprint.



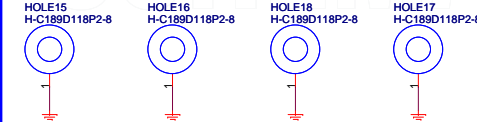
CPU



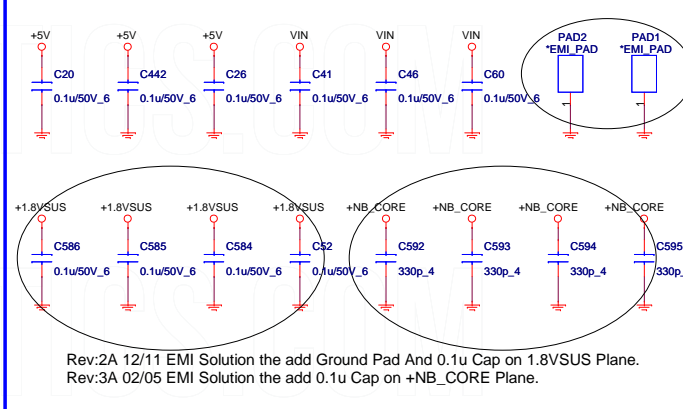
NB



MINI CARD

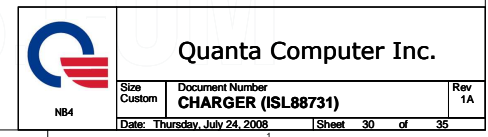


EMI



Quanta Computer Inc.

Size Custom	Document Number KEYBOARD/LED/KILL SW/HOLE	Rev 1A
Date: Thursday, July 24, 2008	Sheet 29	of 35



Rev:2A 12/12 Move the Short Pad.



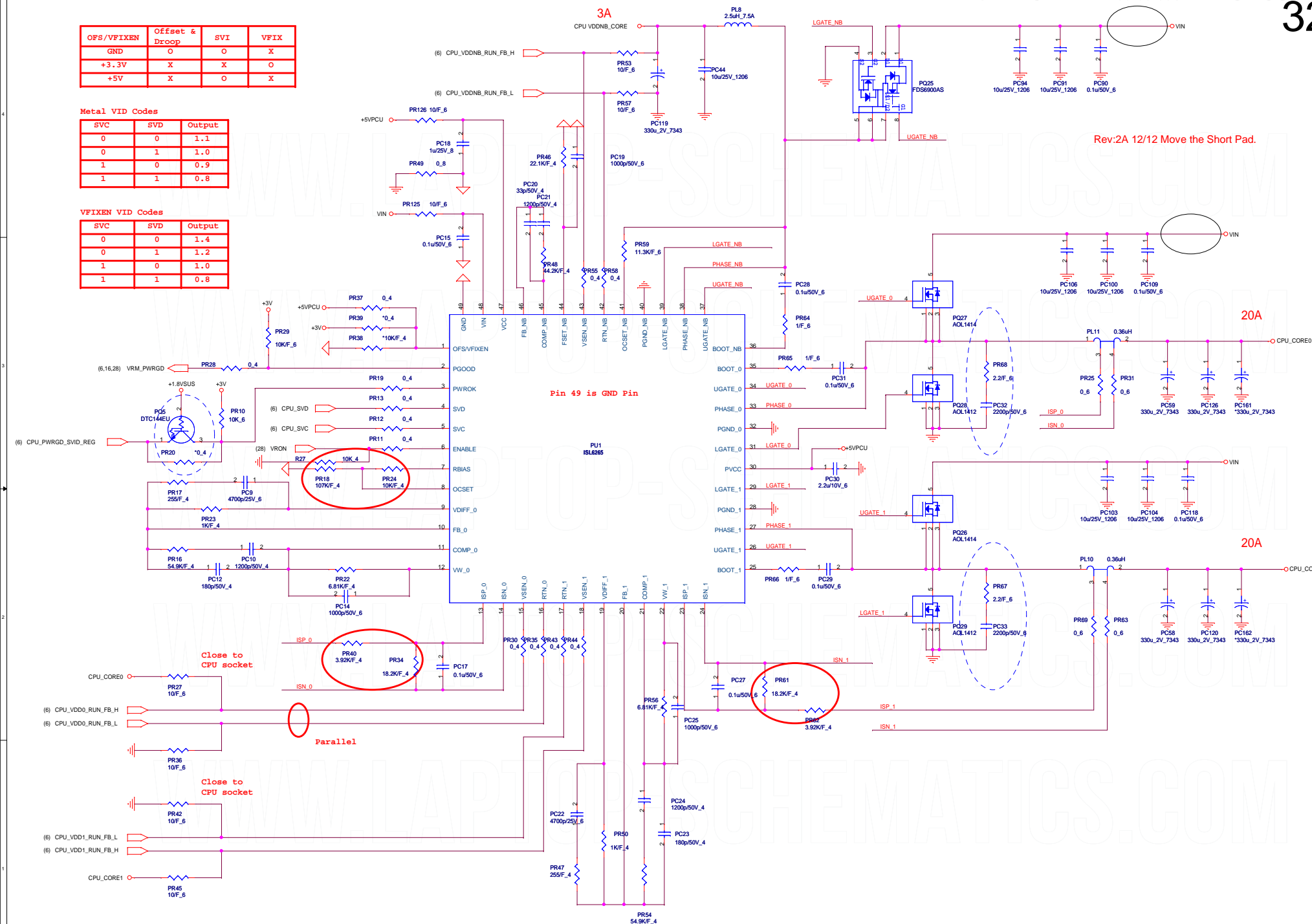
OFS/VFIXEN	Offset & Droop	SVC	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

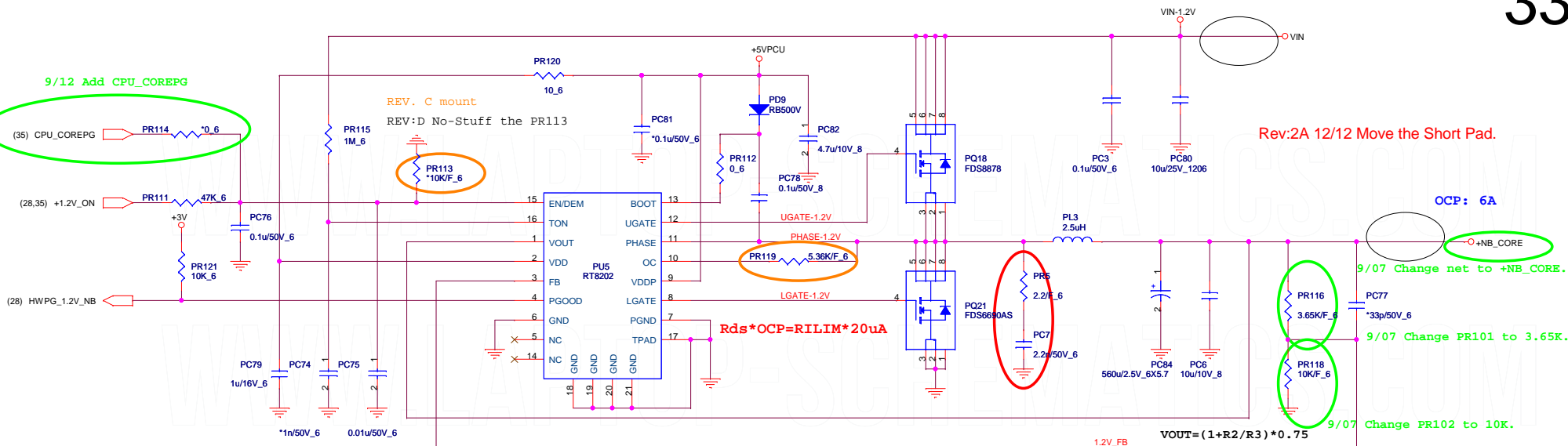
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



Quanta Computer Inc.

Size C	Document Number	Rev 1A
NB4	AMD GRIFFIN CPU (ISL6265)	
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$$TON=3.85p \cdot TON \cdot Vout / (Vin-0.5)$$

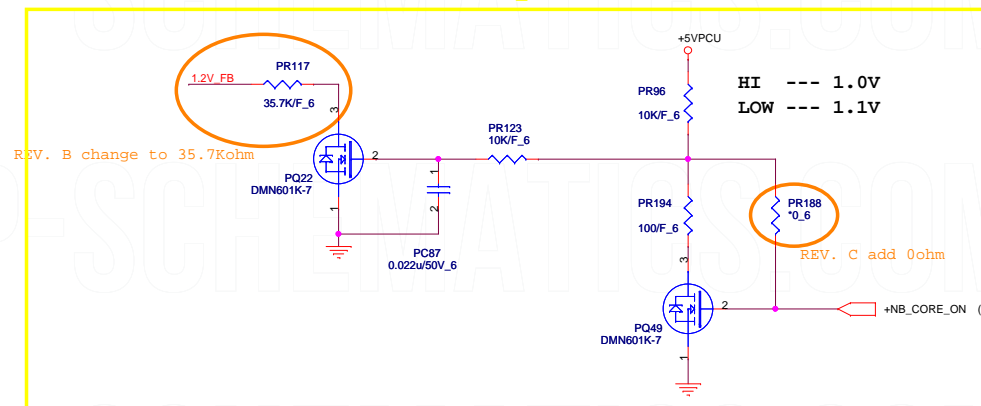
$$6A \text{ OCP} \text{ --- } OC=4.53K$$

$$FDS6690AS \text{ Rds}=15mOhm$$

$$Frequency=Vout / (Vin \cdot TON)$$

REV. C PR119 change to 5.36Kohm

1/30 modify



9/07 Change net to +NB_CORE.

9/12 Addition PR156, PQ43.

