

Compal Confidential

Picard-1 PILP1 LA-6921P Schematics Document

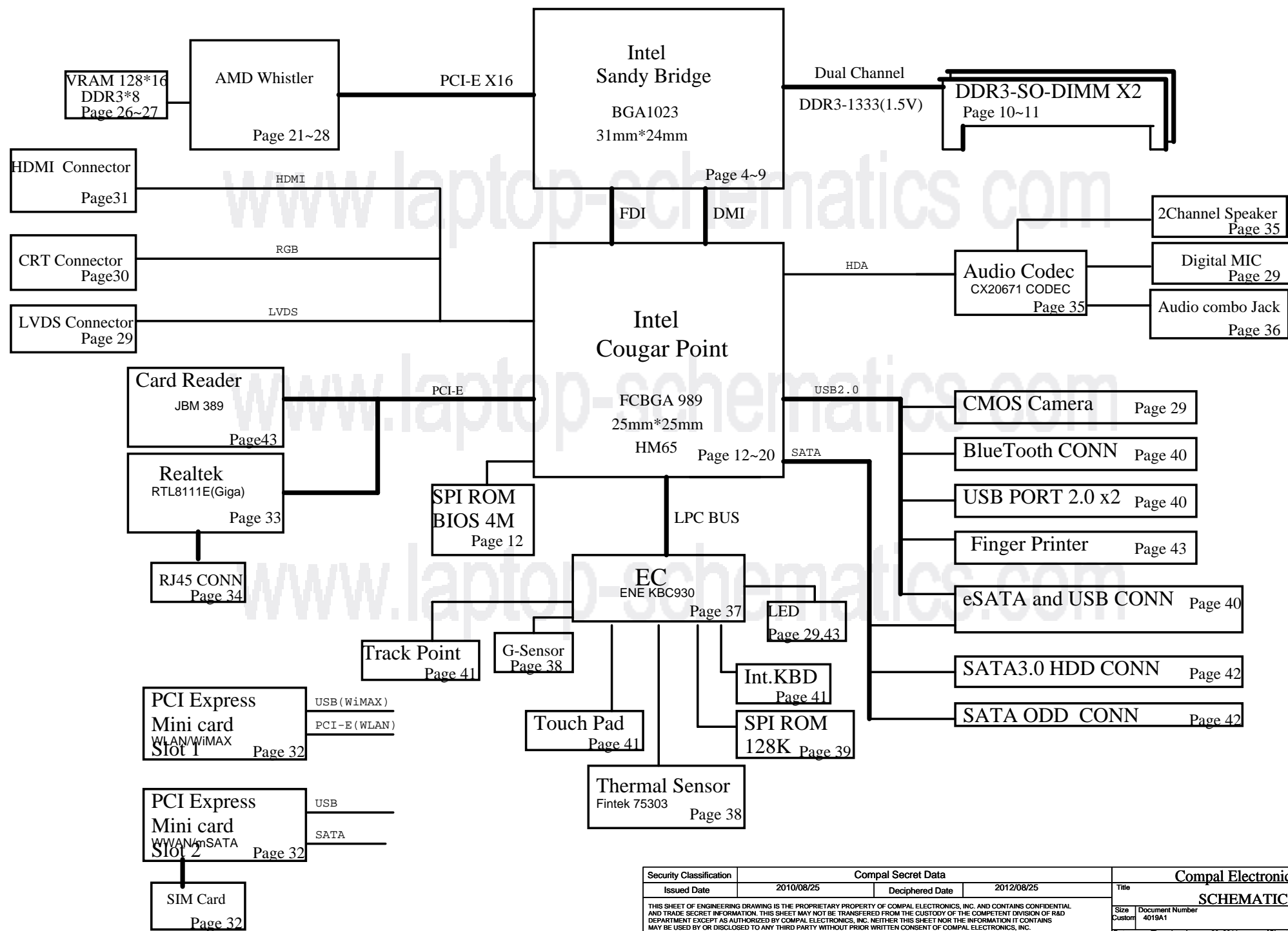
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH + Whistler 128bit with BACO

2010-12-12

REV:1.0

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Picard-1 PILP1 LA-6921P Block Diagram



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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +VGFX_CORE +CPU_CORE +0.75VS +1.5VS_DISVGA +1.0VS +NVVDD +3VS_DISVGA +1.8VS_DISVGA
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	X	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB_COMBO
		1	USB_PORT
	UHCI1	2	NO USE
		3	NO USE
	UHCI2	4	WWAN
		5	CAMERA
EHCI2	UHCI3	6	HM65 not support
		7	HM65 not support
	UHCI4	8	WLAN
		9	USB_CHARGER
	UHCI5	10	NO USE
		11	NO USE
	UHCI6	12	FINGER-PRINTER
		13	BLUETOOTH

BOM Structure Table

Structure	Function
CPU1@	CPU type
PX@	PX4.0 SKU
UMA@	UMA SKU
3G@	3G Sim card
X76H1G@	VRAM
PCB@	M/B

Vcc	3.3V +/- 5%				
R613	100K +/- 5%				
Board ID	R682	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0K +/- 5%	0 V	0 V	0 V	SDV1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SVT

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	1	0	PX4.0

ZZZ1	ZZZ2	ZZZ3	ZZZ4	ZZZ5
PCB@ LA-6921P DA8000L700	X76H2G@ HYNIX_2G X762603BL01	X76S2G@ SAMSUNG_2G X762603BL02	X76H1G@ HYNIX_1G X762603BL03	X76S1G@ SAMSUNG_1G X762603BL04

UCPU1	UCPU1	UCPU1	UCPU1	UCPU1
CPU2@ i3-2310M 2.1G Q1R1K SA00004KP00	CPU3@ i5-2410M 2.3G Q1R9 SA00004KT00	CPU4@ i5-2520M 2.5G Q1RA SA00004EL20	CPU5@ i5-2540M 2.6G Q1R7 SA00004EM20	CPU6@ i7-2620M 2.7G Q1R3 SA00004F010

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

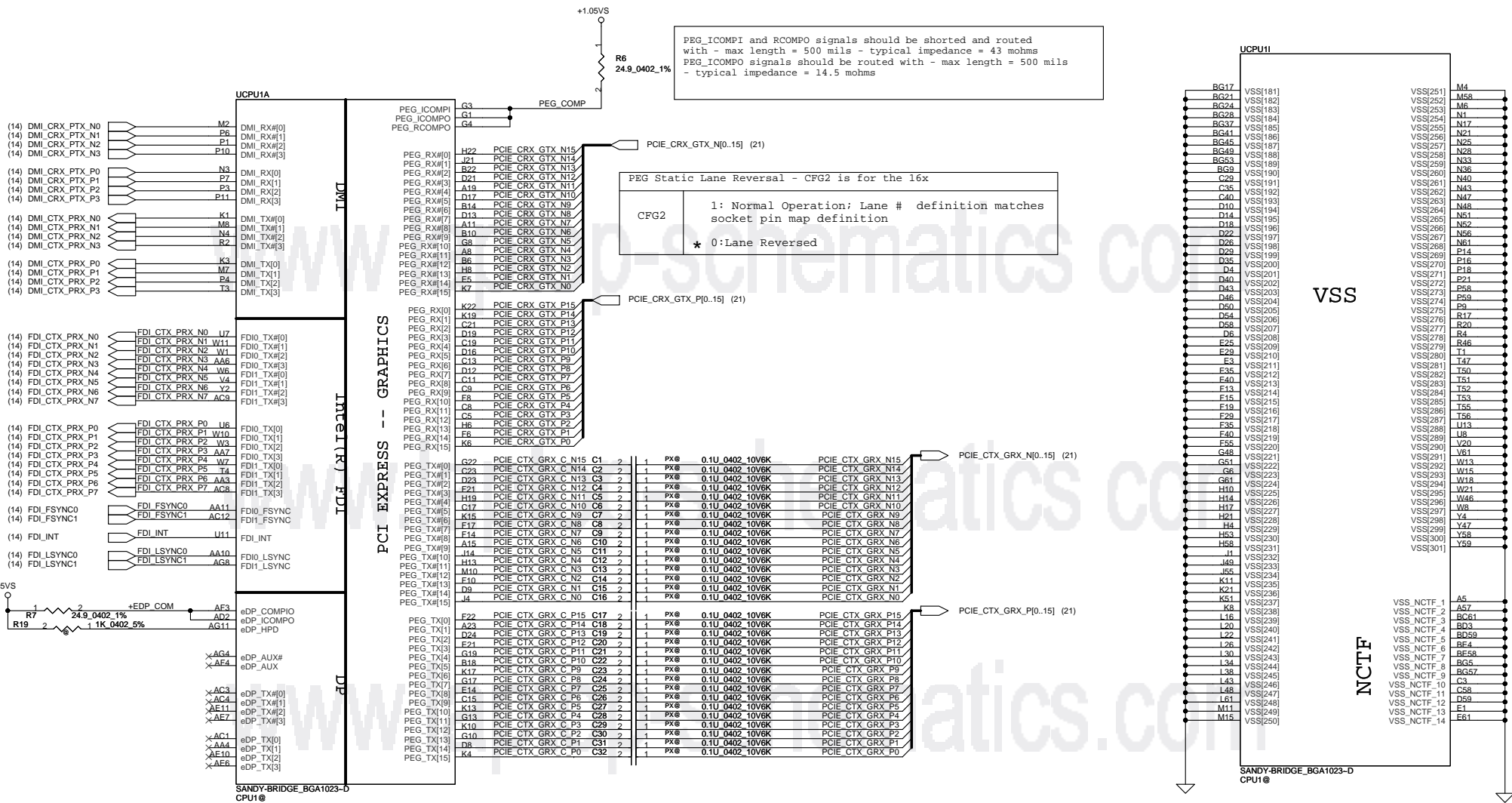
EC SM Bus2 address

Device	Address
PCH	1001 0110 b
Thermal sensor(U30)	1001 101x b
GPU(U9)	1000_0010 b

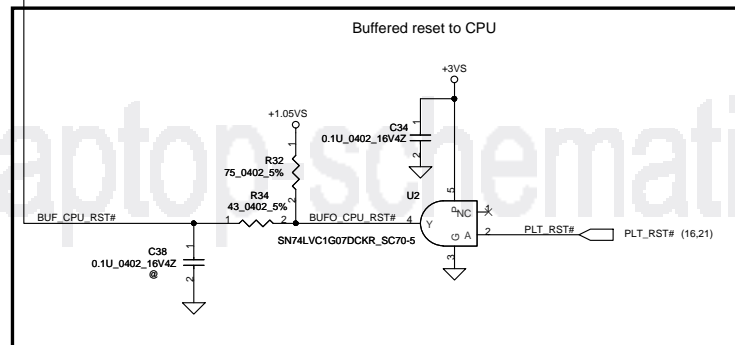
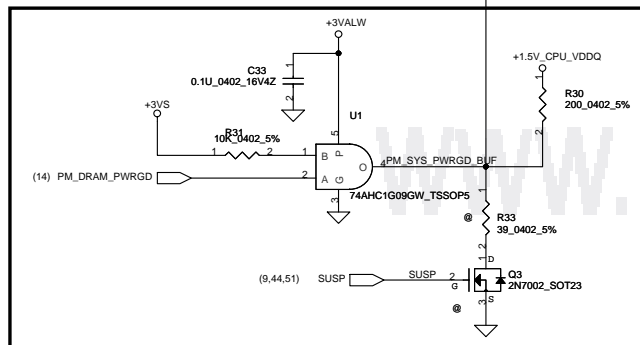
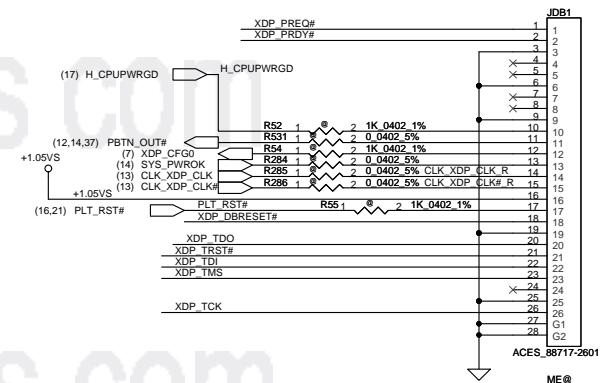
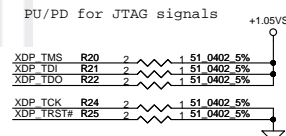
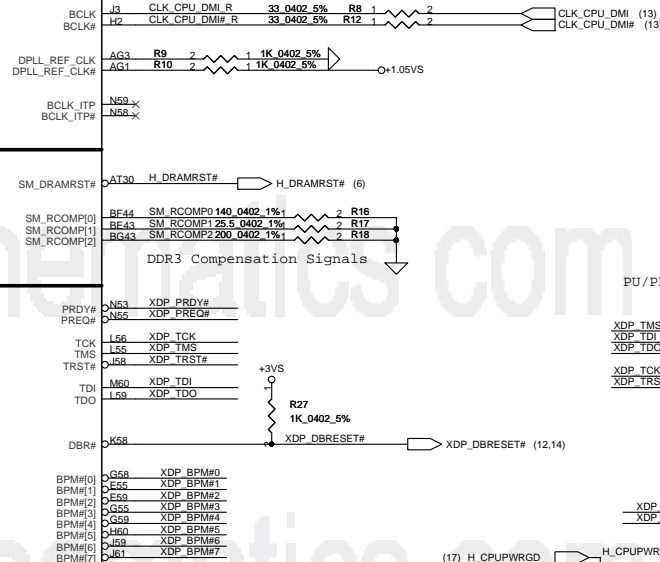
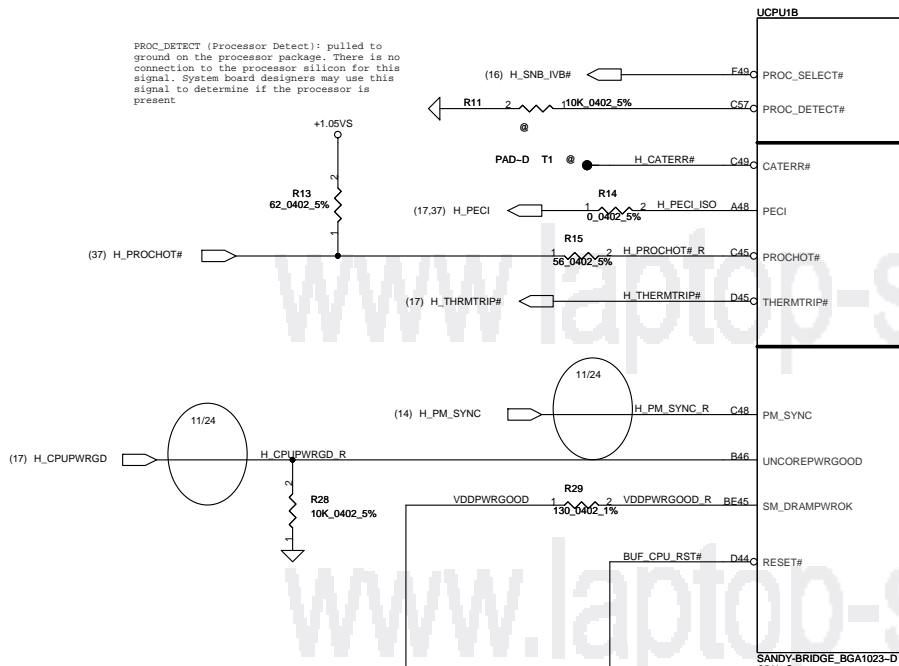
PCH SM Bus address

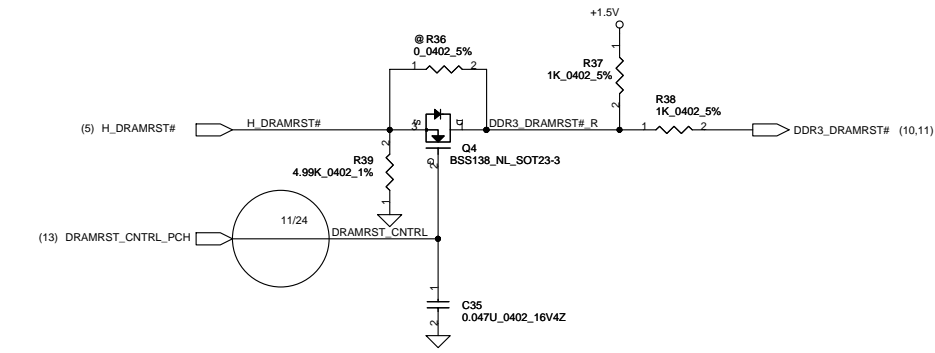
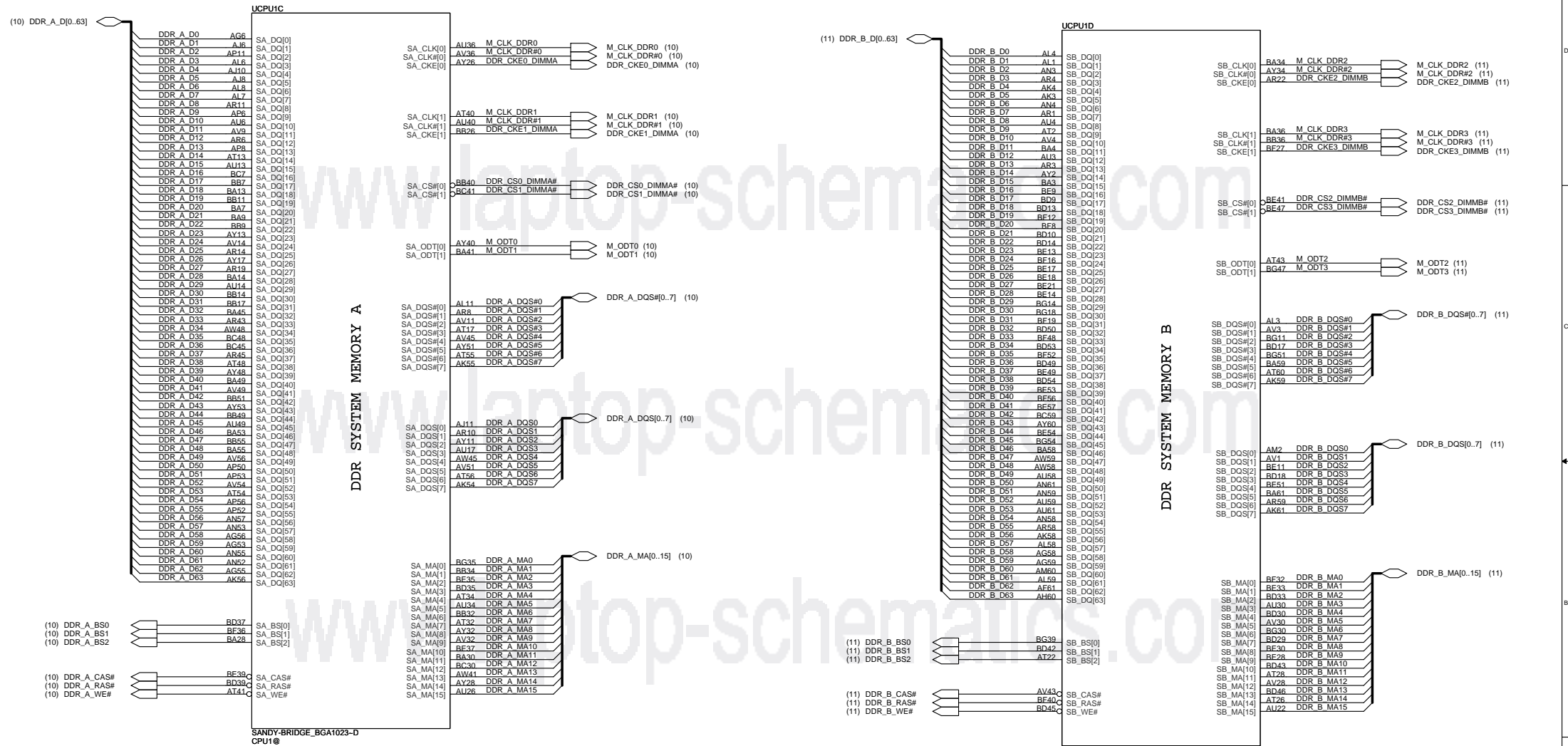
Device	Address
DDR DIMM0	1010 000xb
DDR DIMM2	1010 010xb
EEPROM(U32)	1010 100xb

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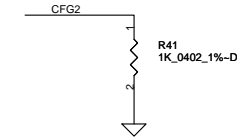
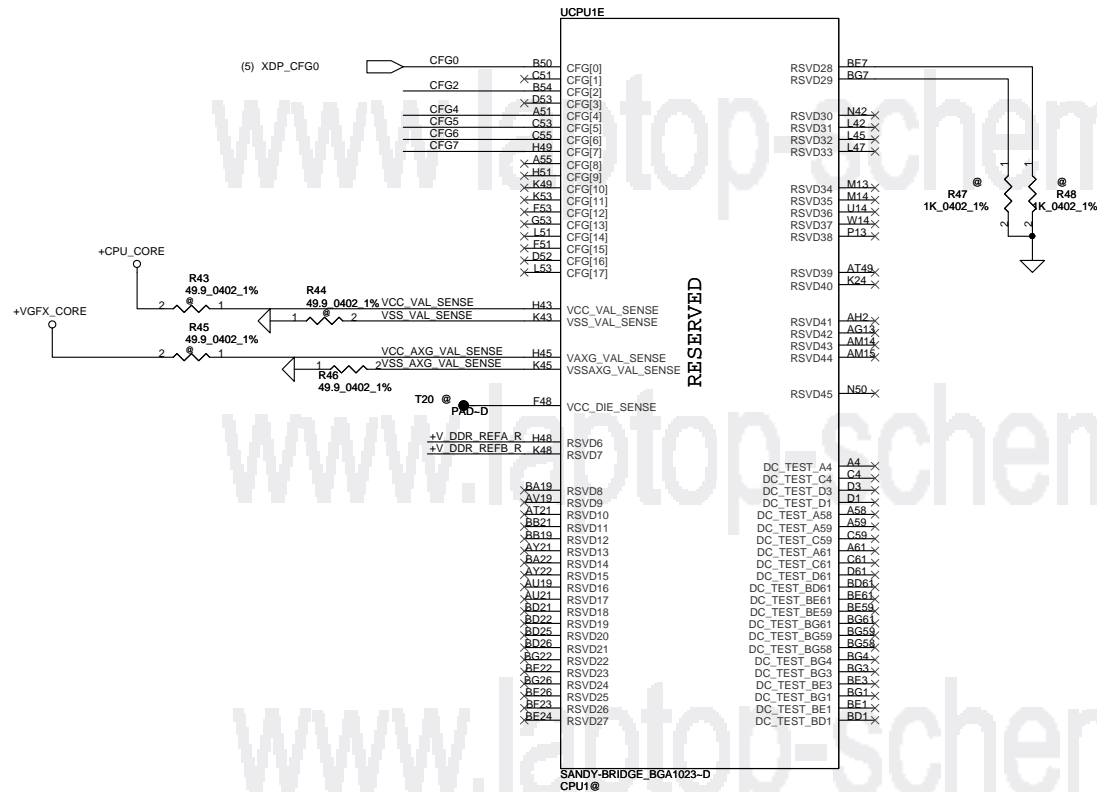
PROC_DETECT# (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.



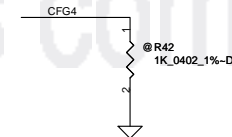


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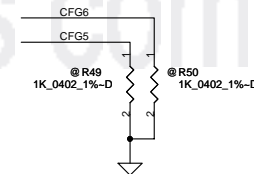
CFG Straps for Processor



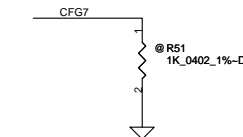
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



Display Port Presence Strap	
CFG4	<p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

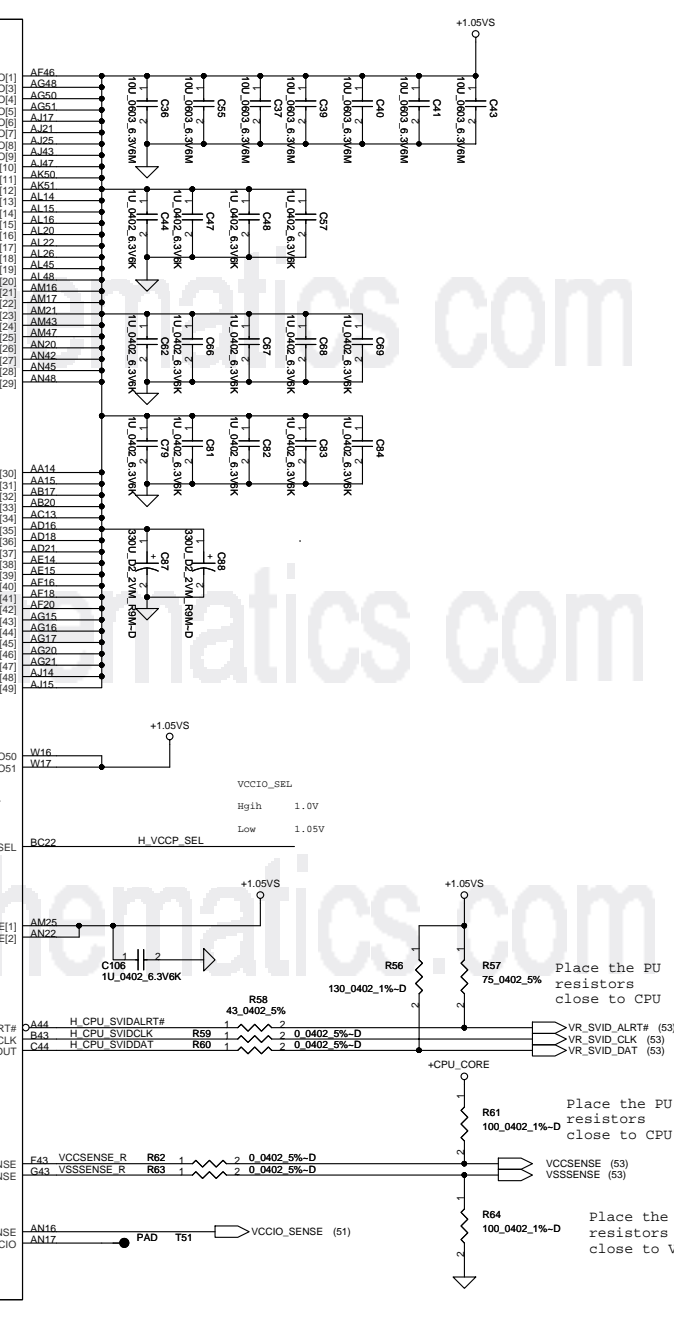
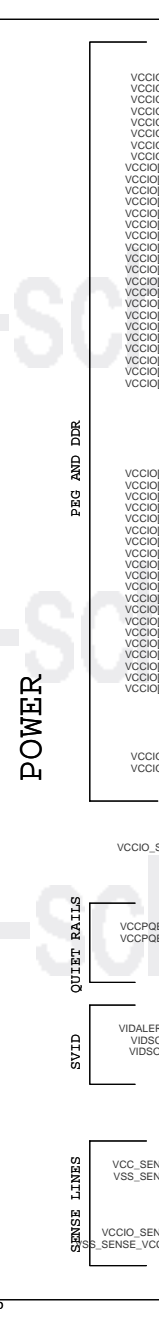
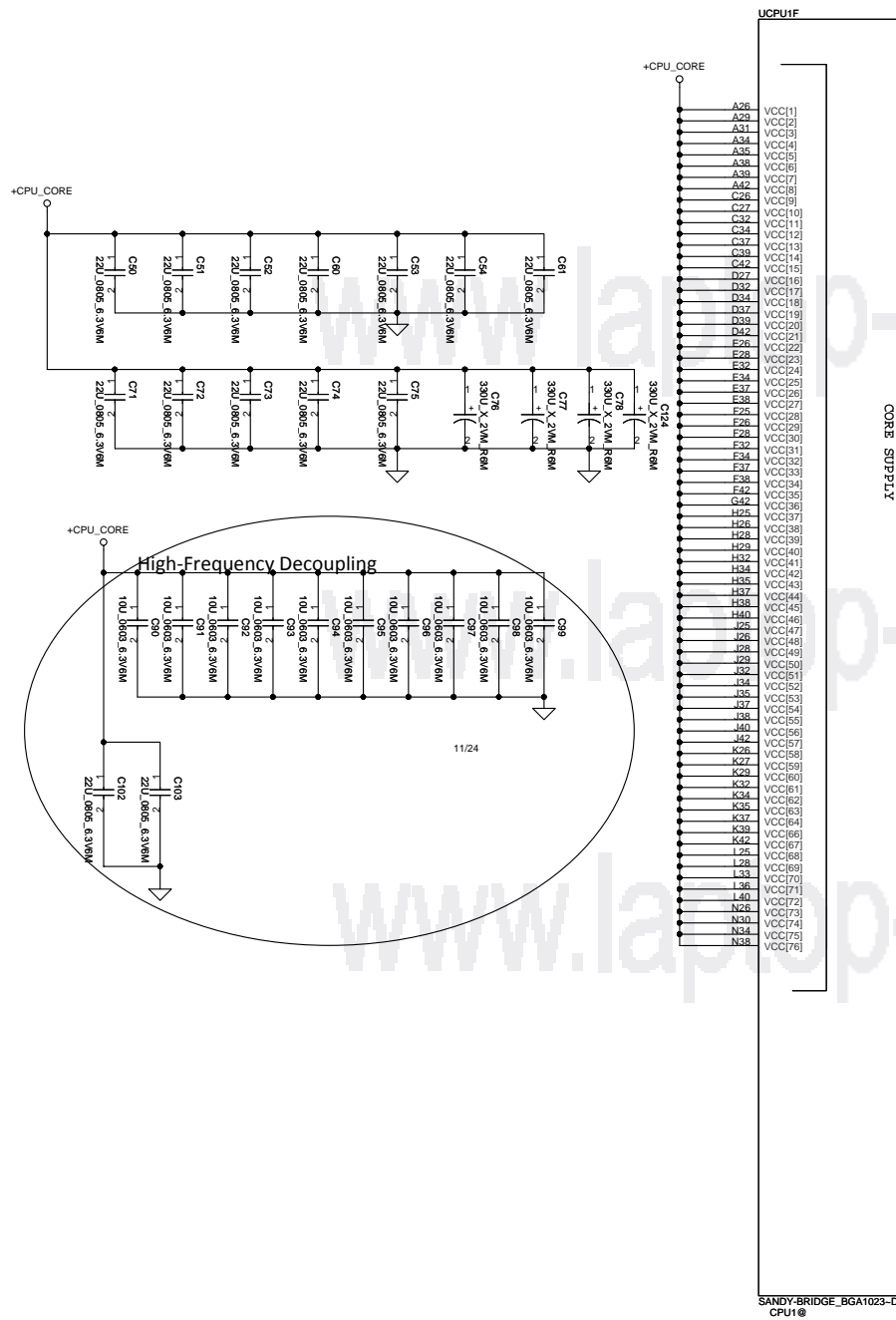


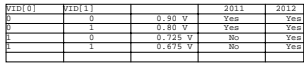
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



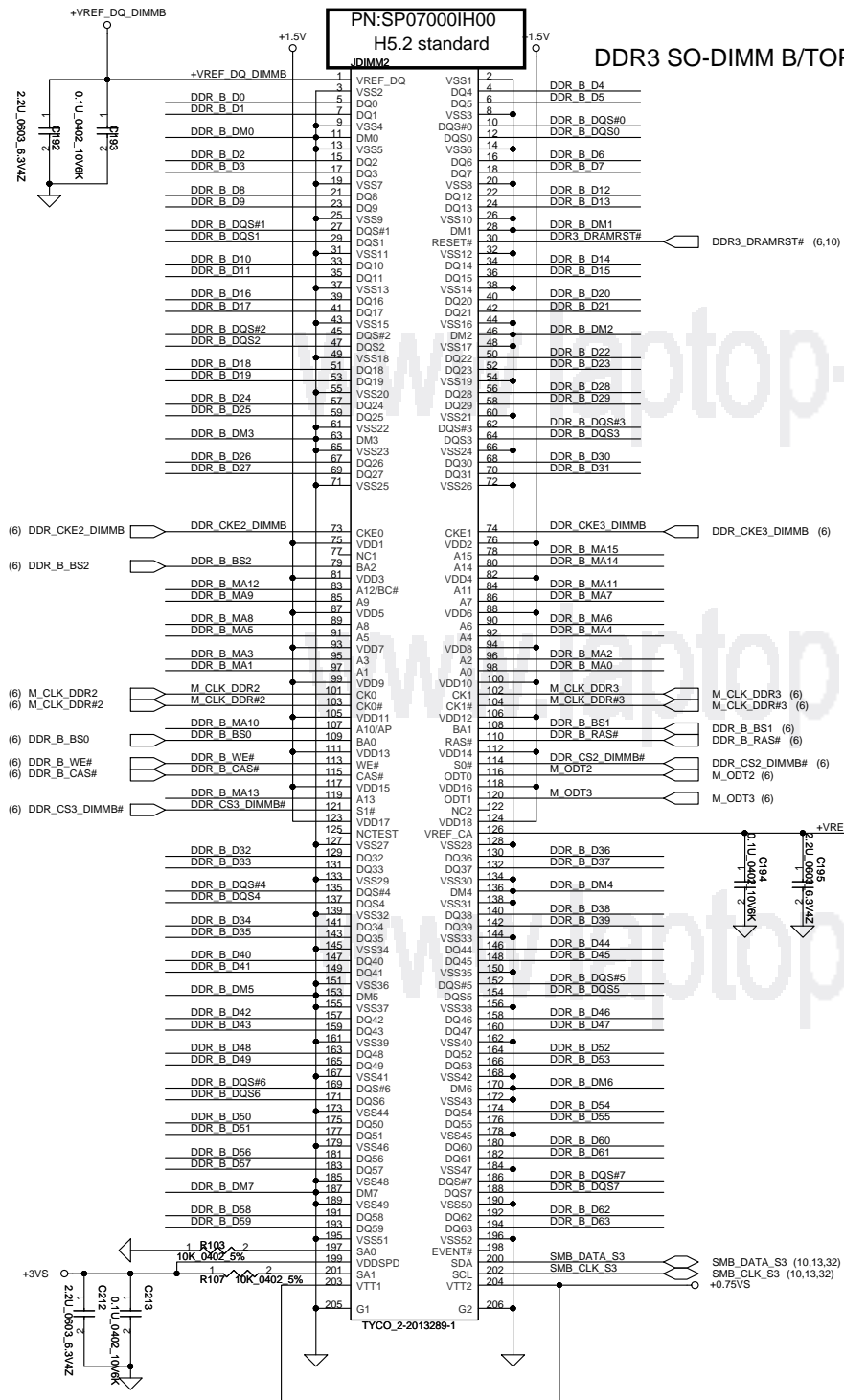
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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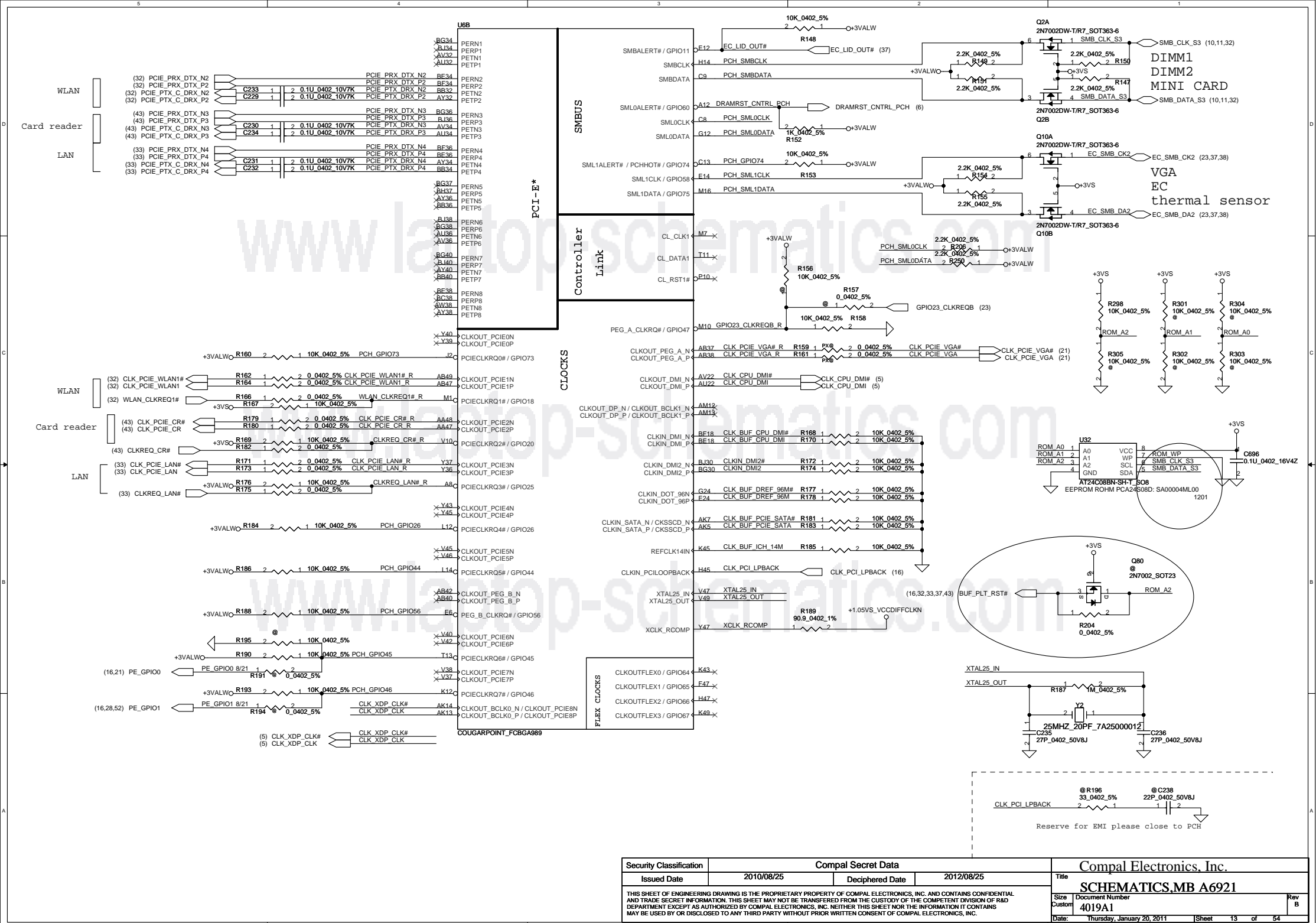


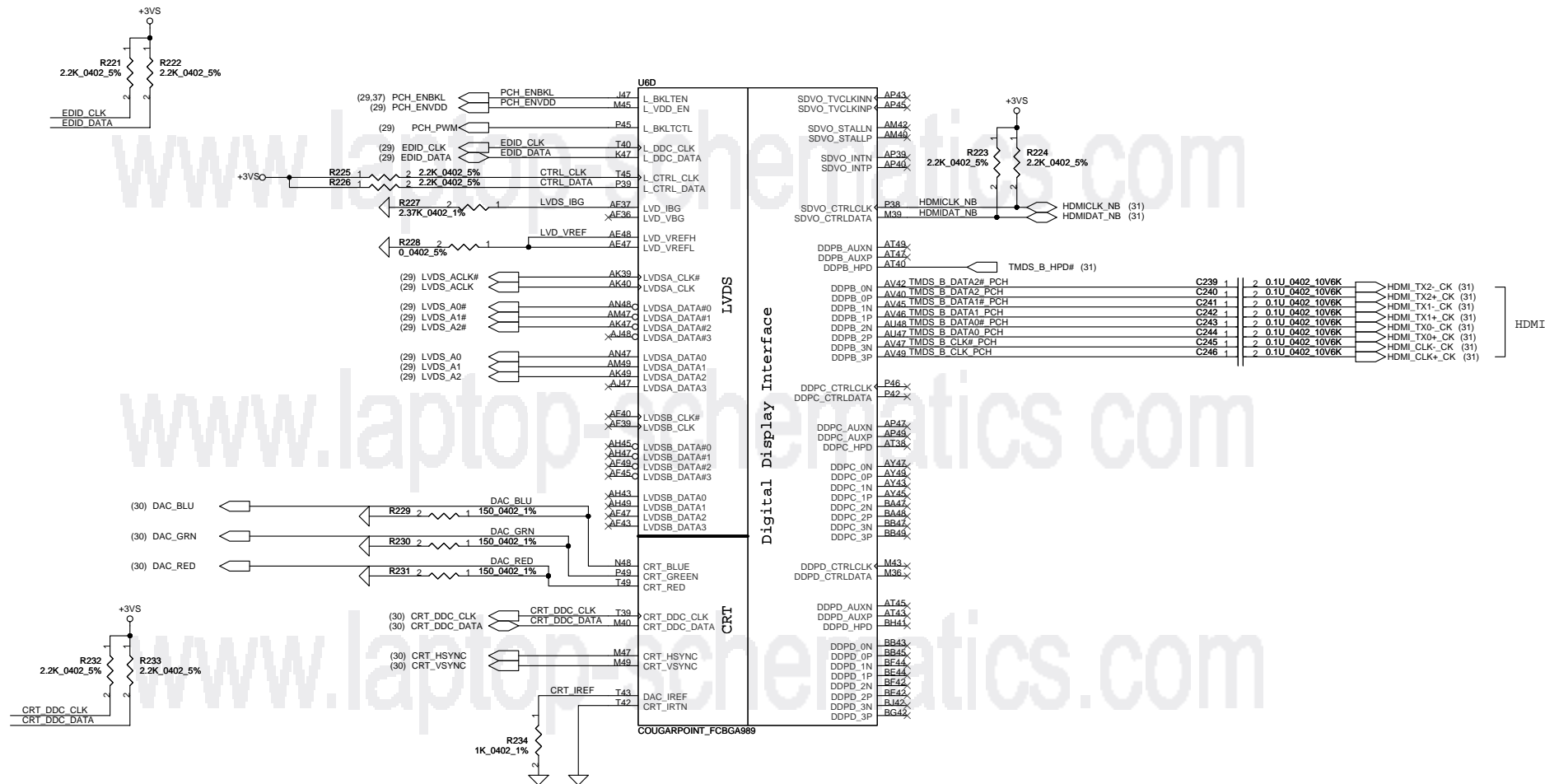


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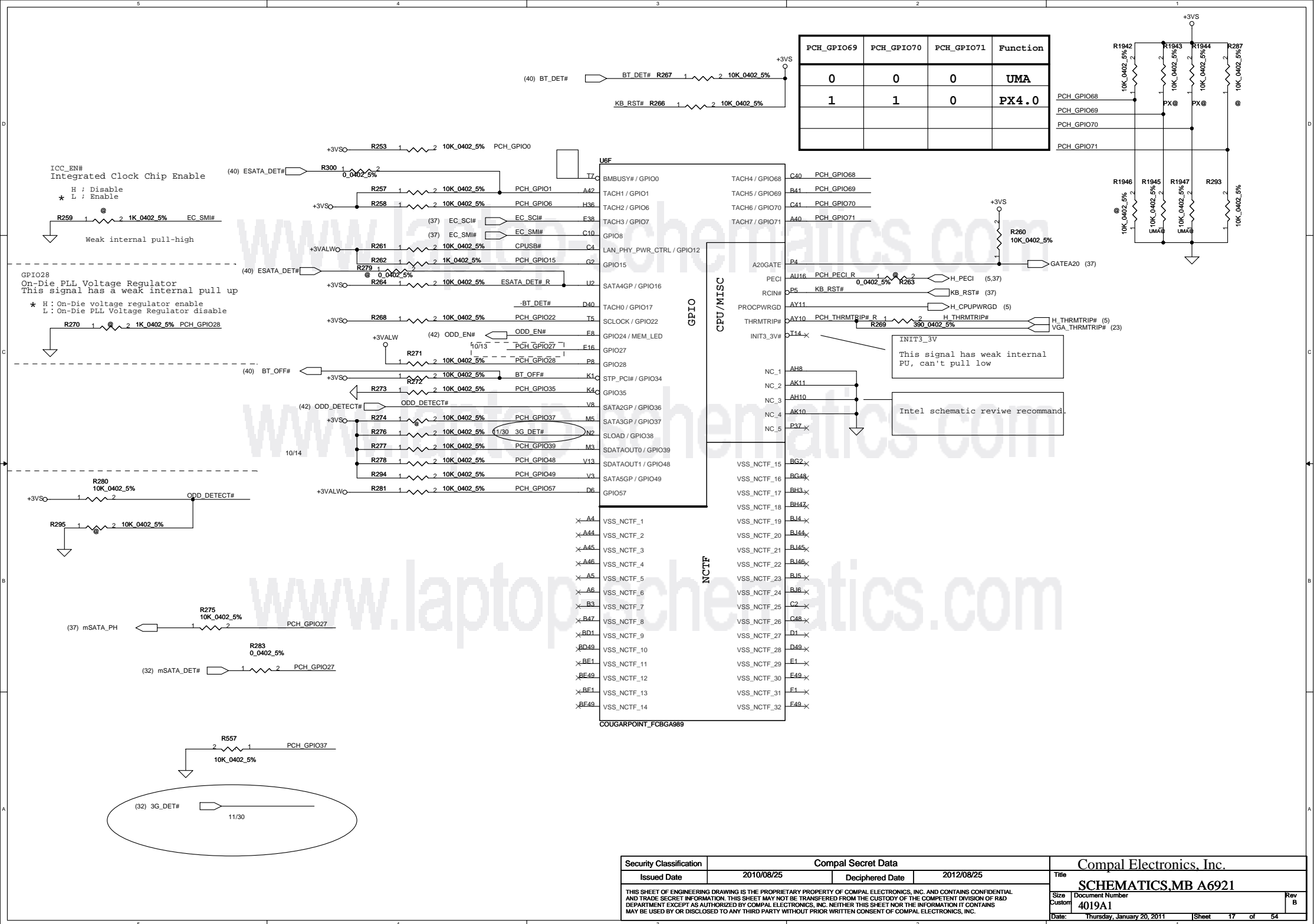


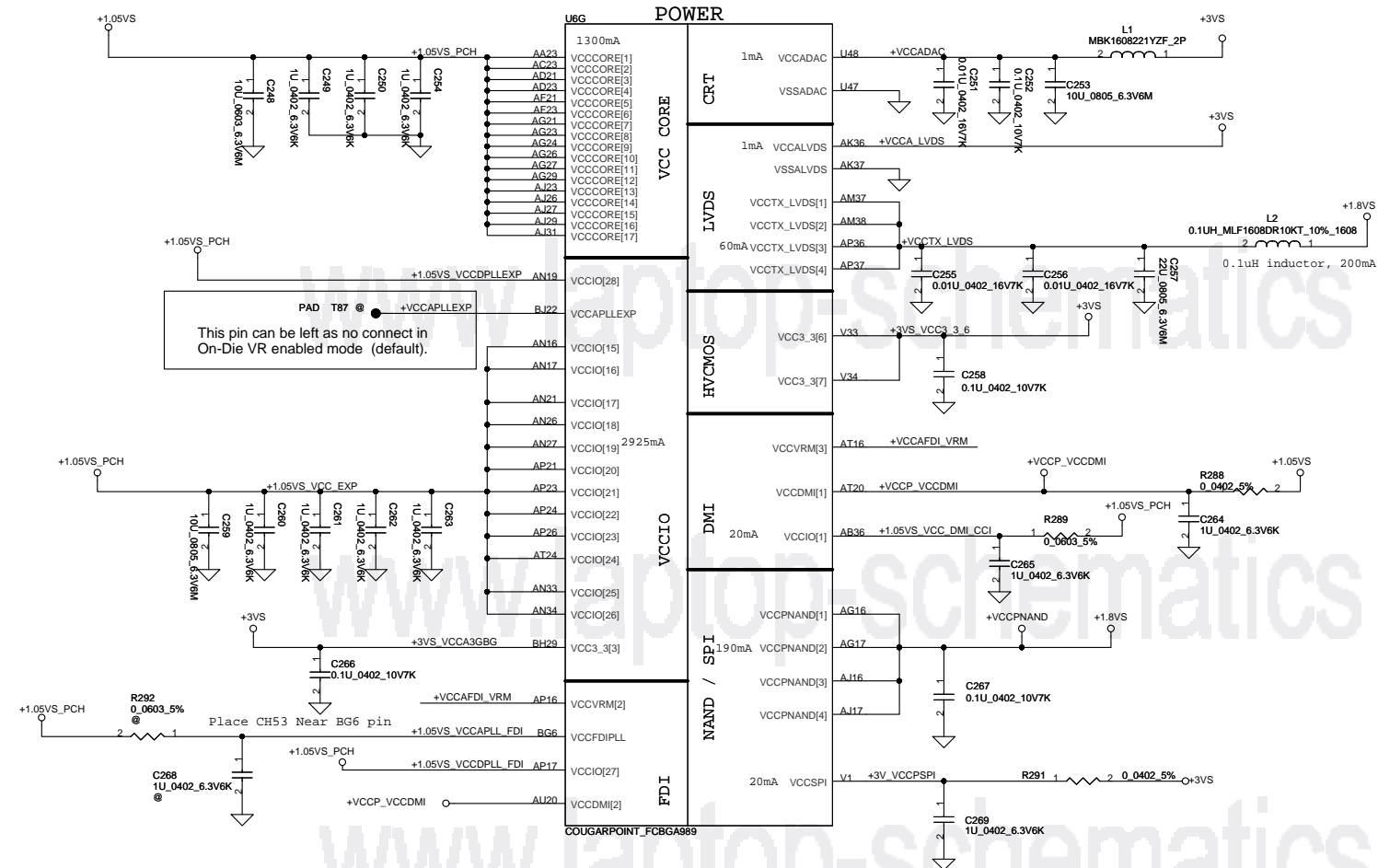
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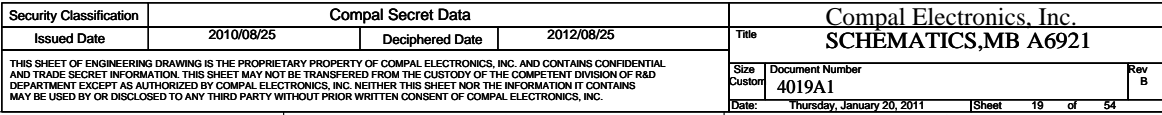


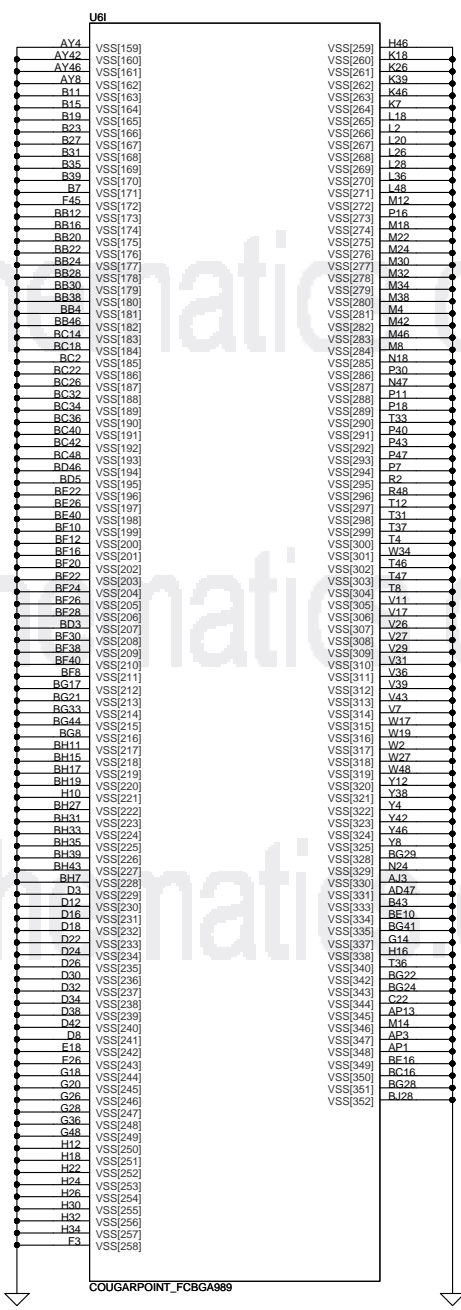
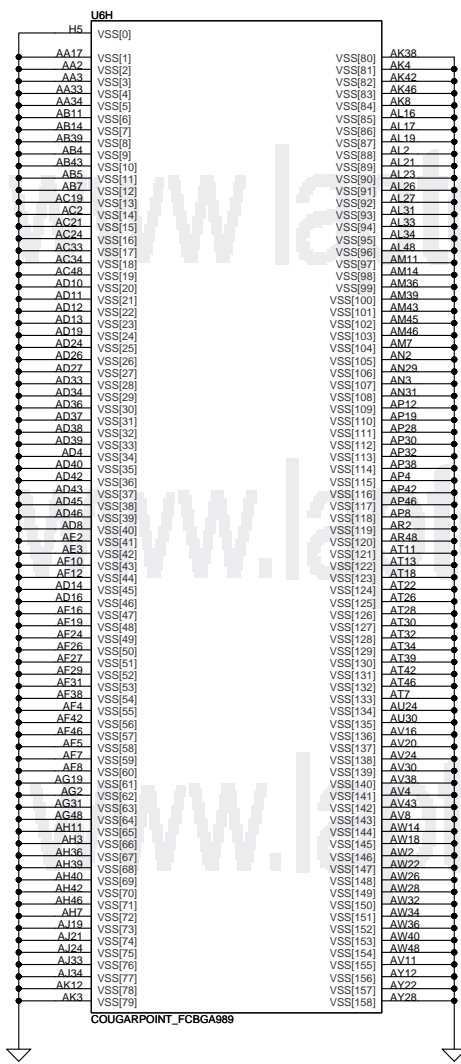
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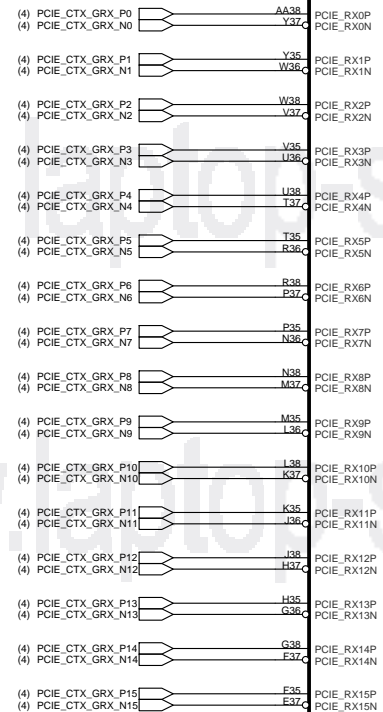
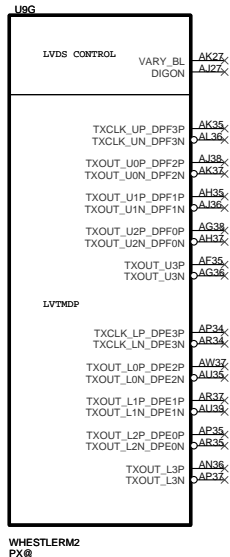
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



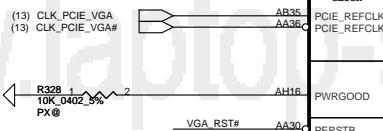
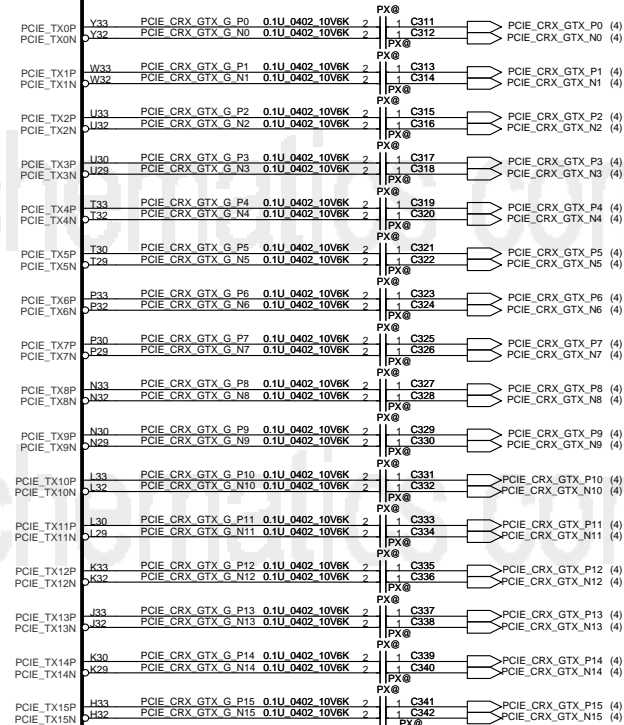


PEG Interface

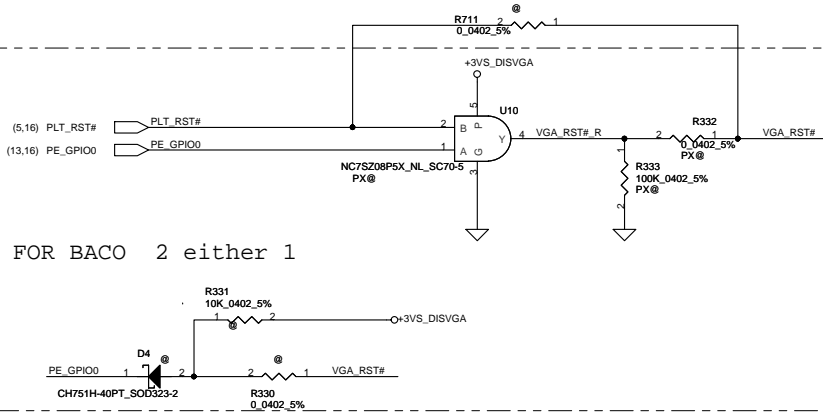
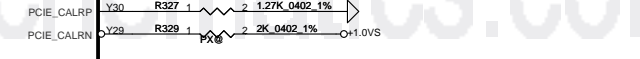
LVDS Interface



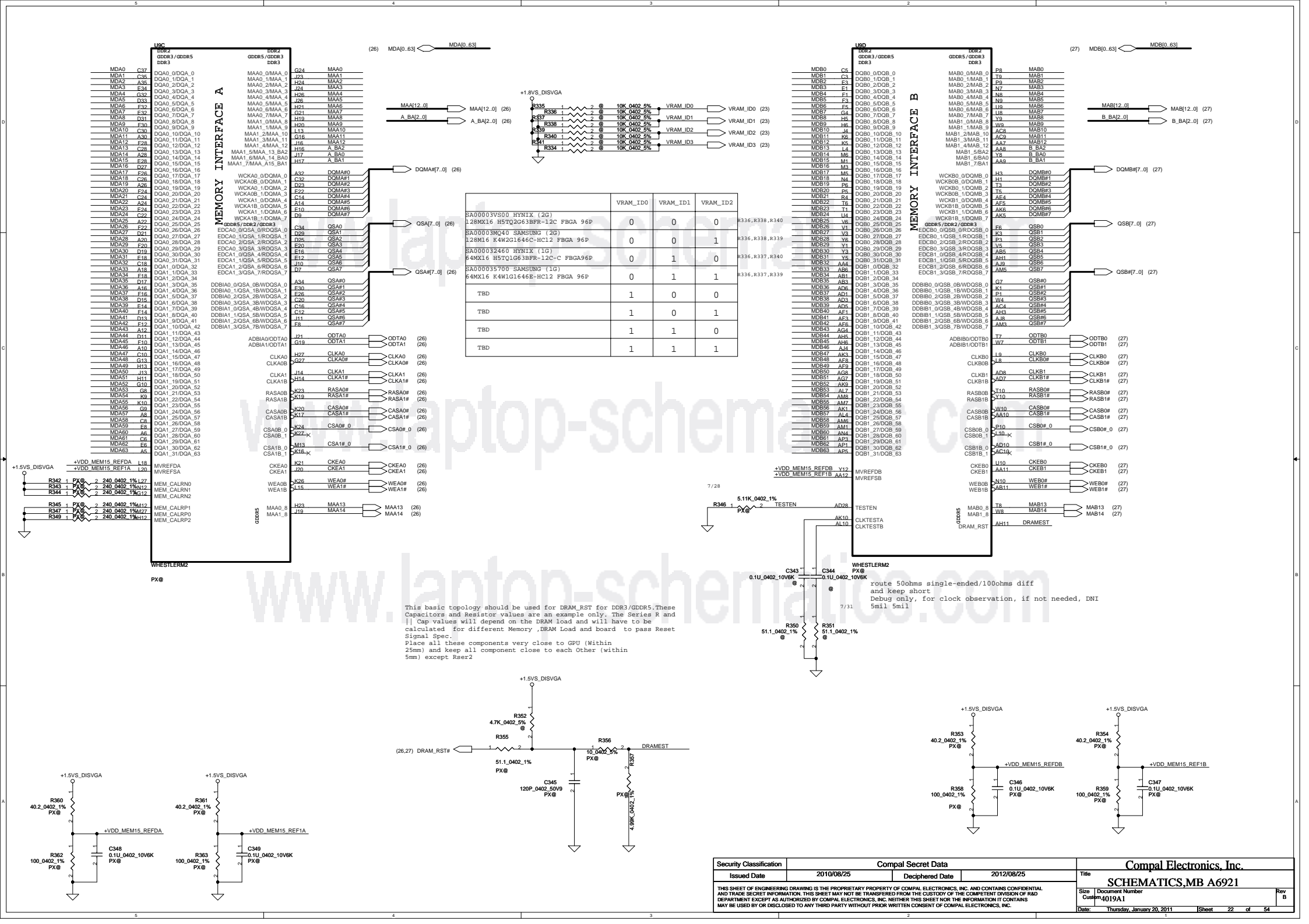
PCI EXPRESS INTERFACE

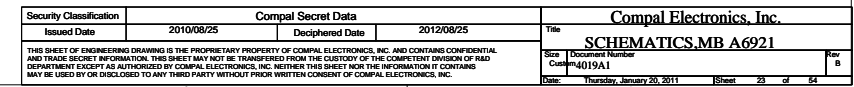


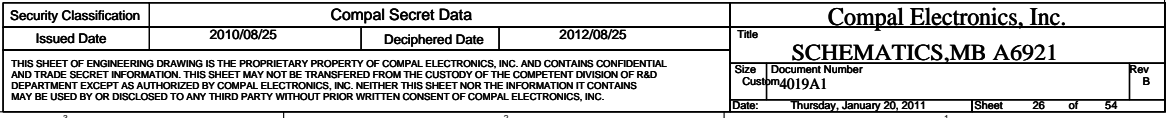
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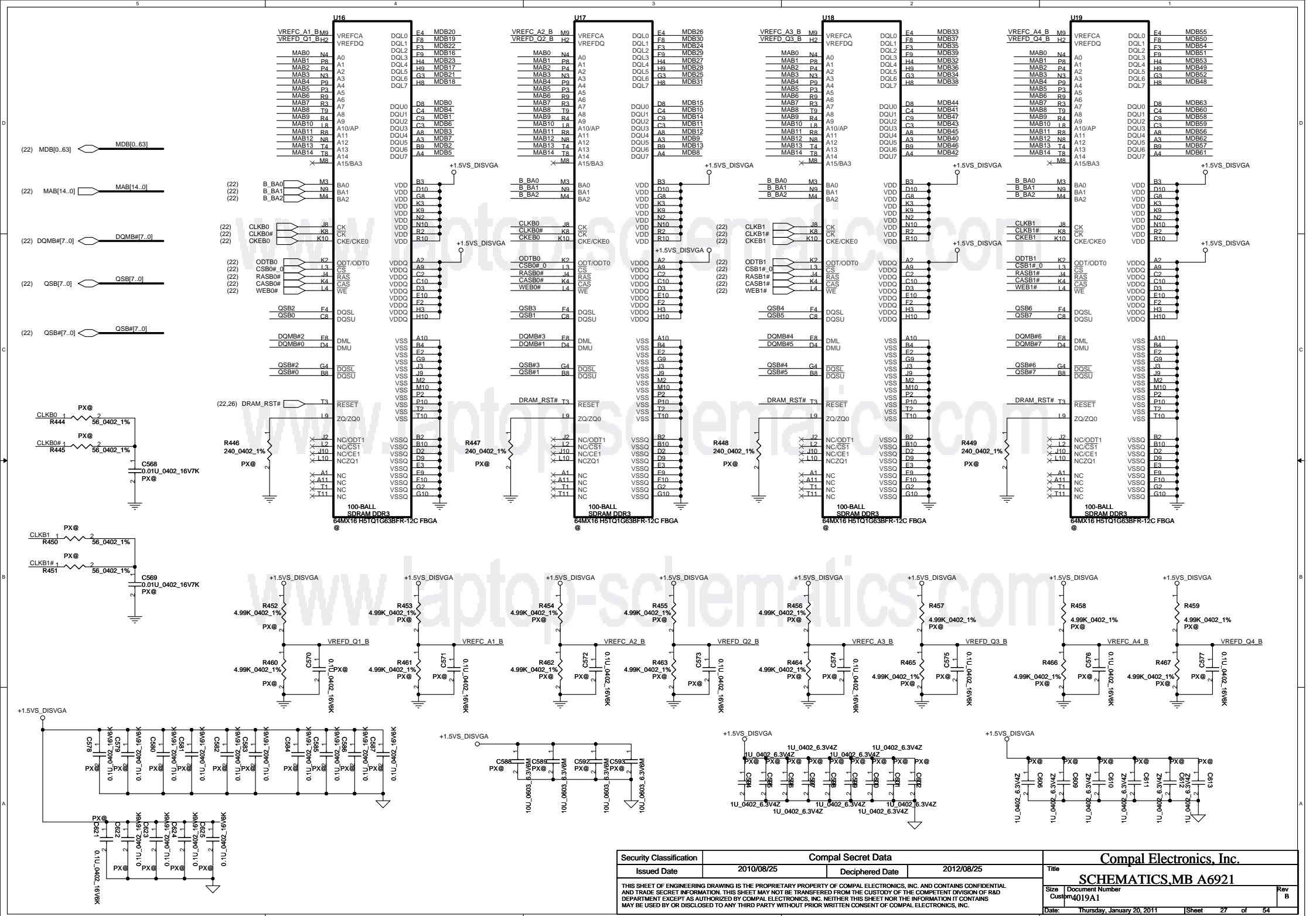


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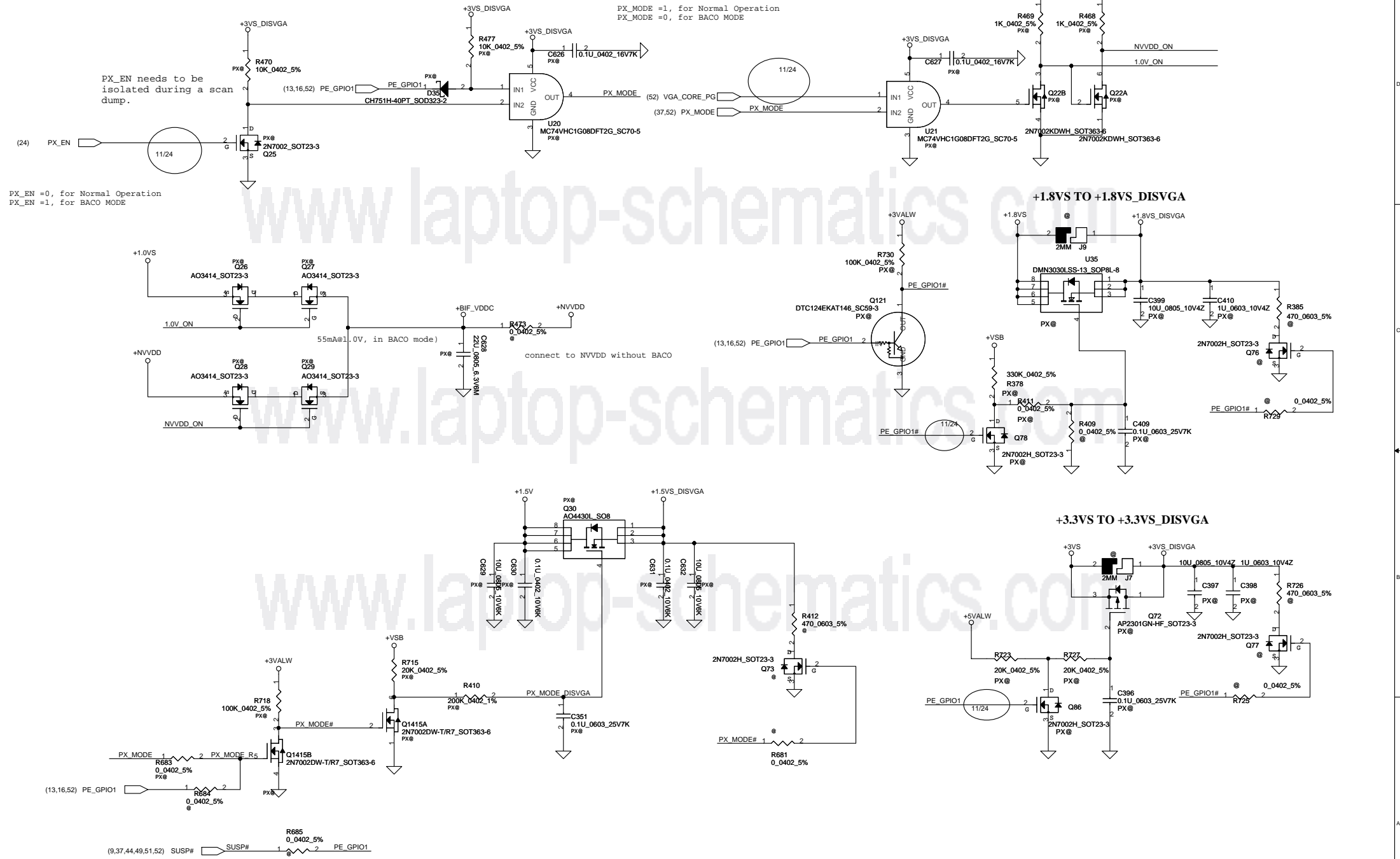






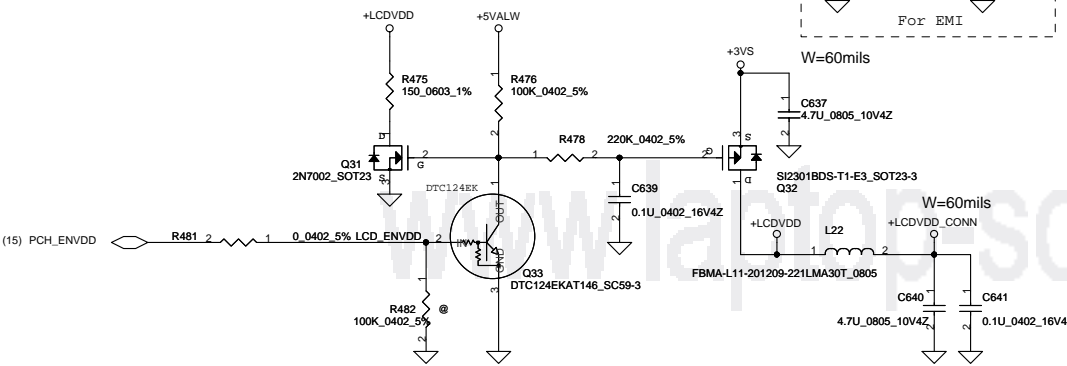


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LCD POWER CIRCUIT

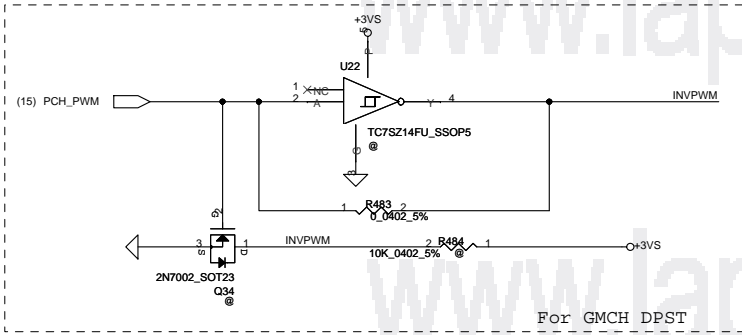


W=60mils

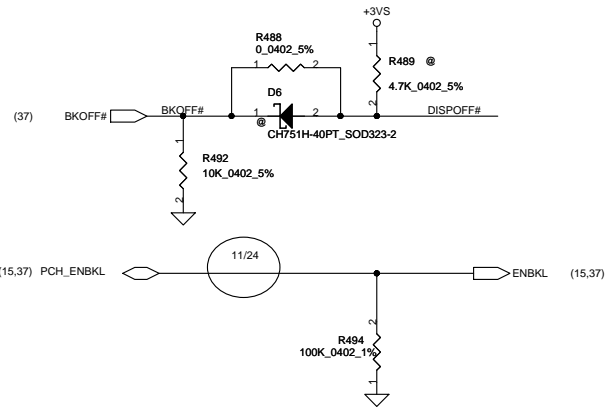
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(43) TL_LED#

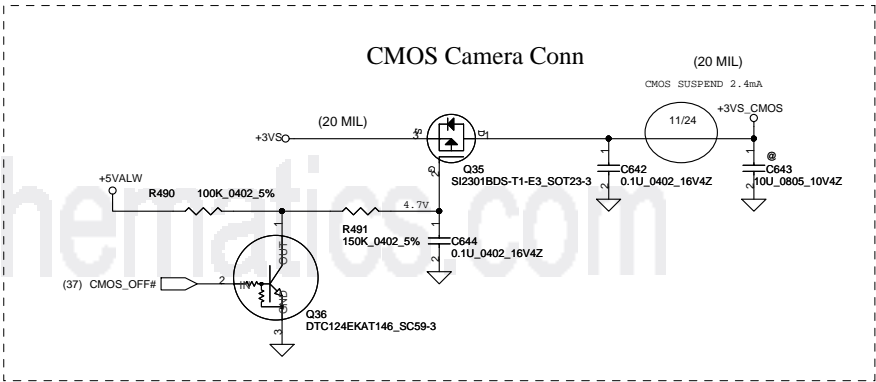
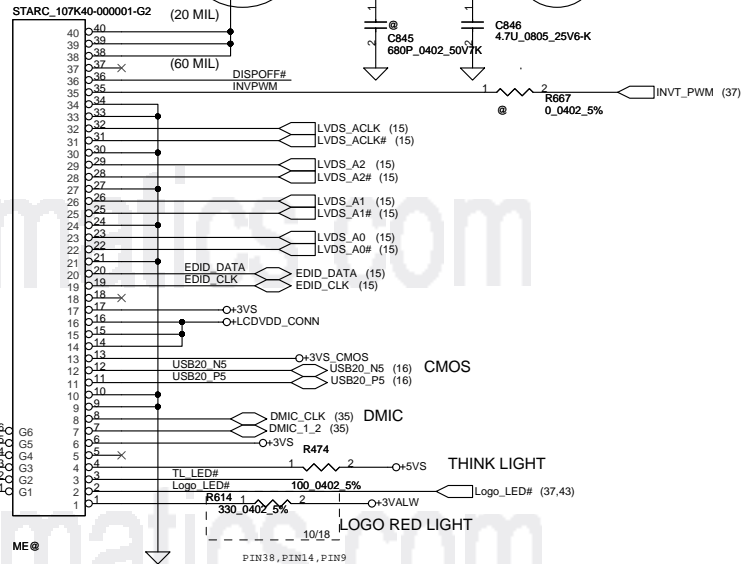
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For GMCH DPST



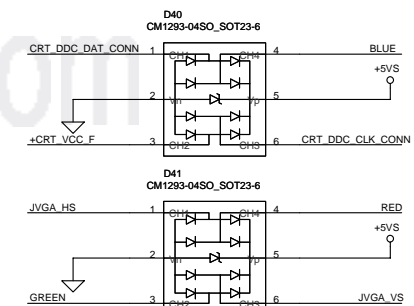
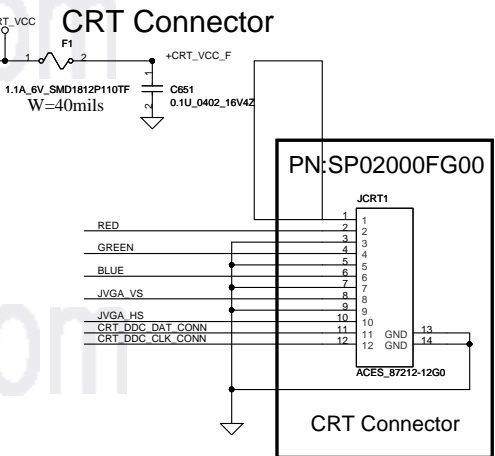
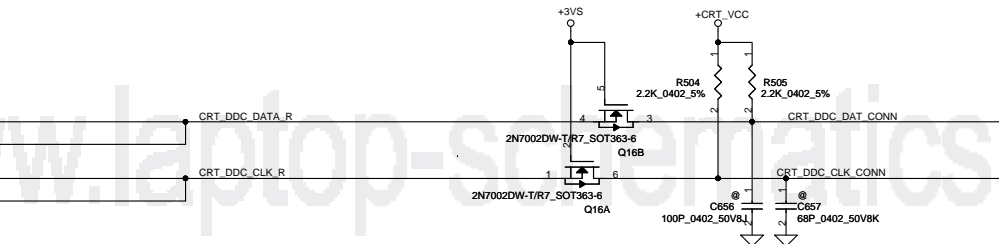
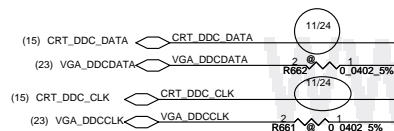
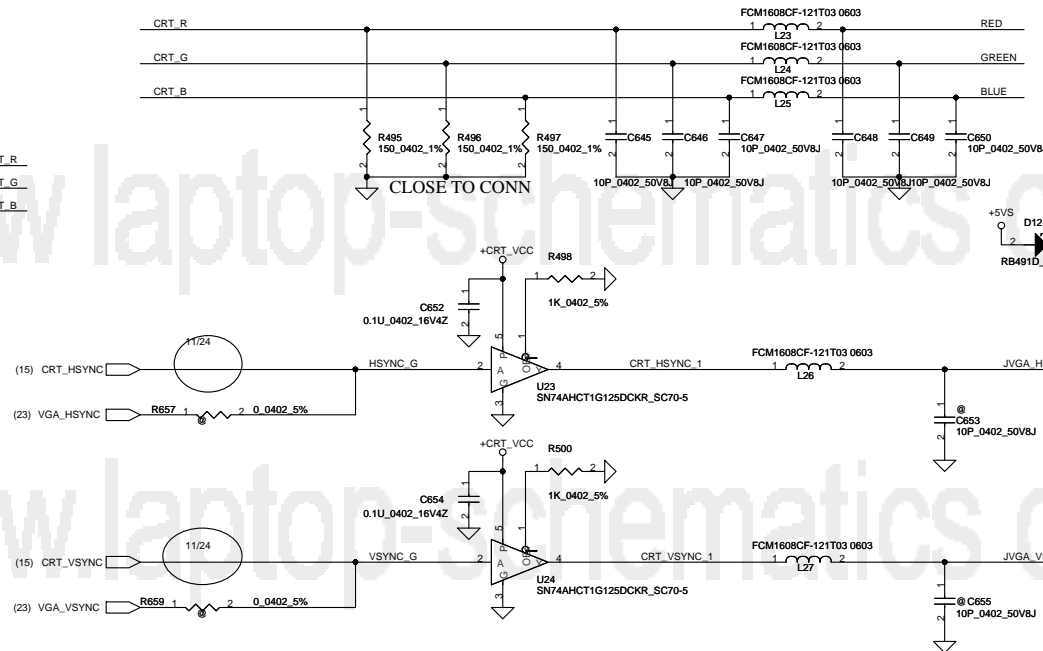
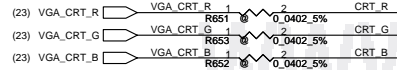
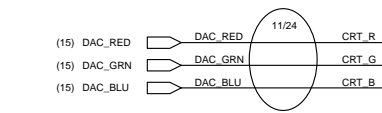
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JLCD1



CMOS Camera Conn

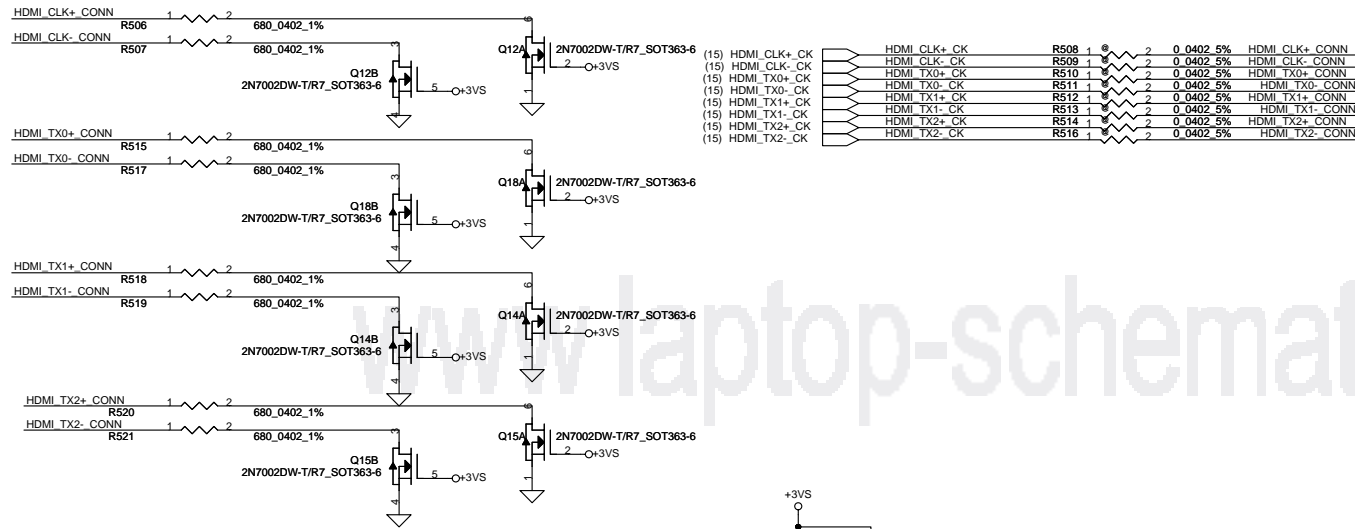
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								Document Number			
								4019A1			
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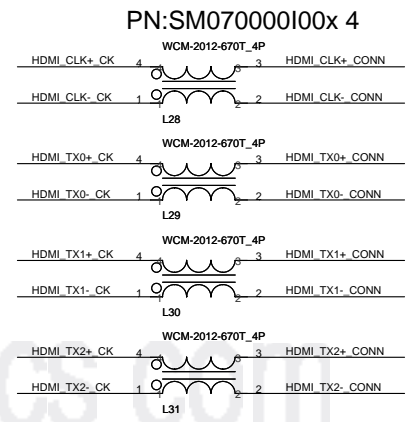


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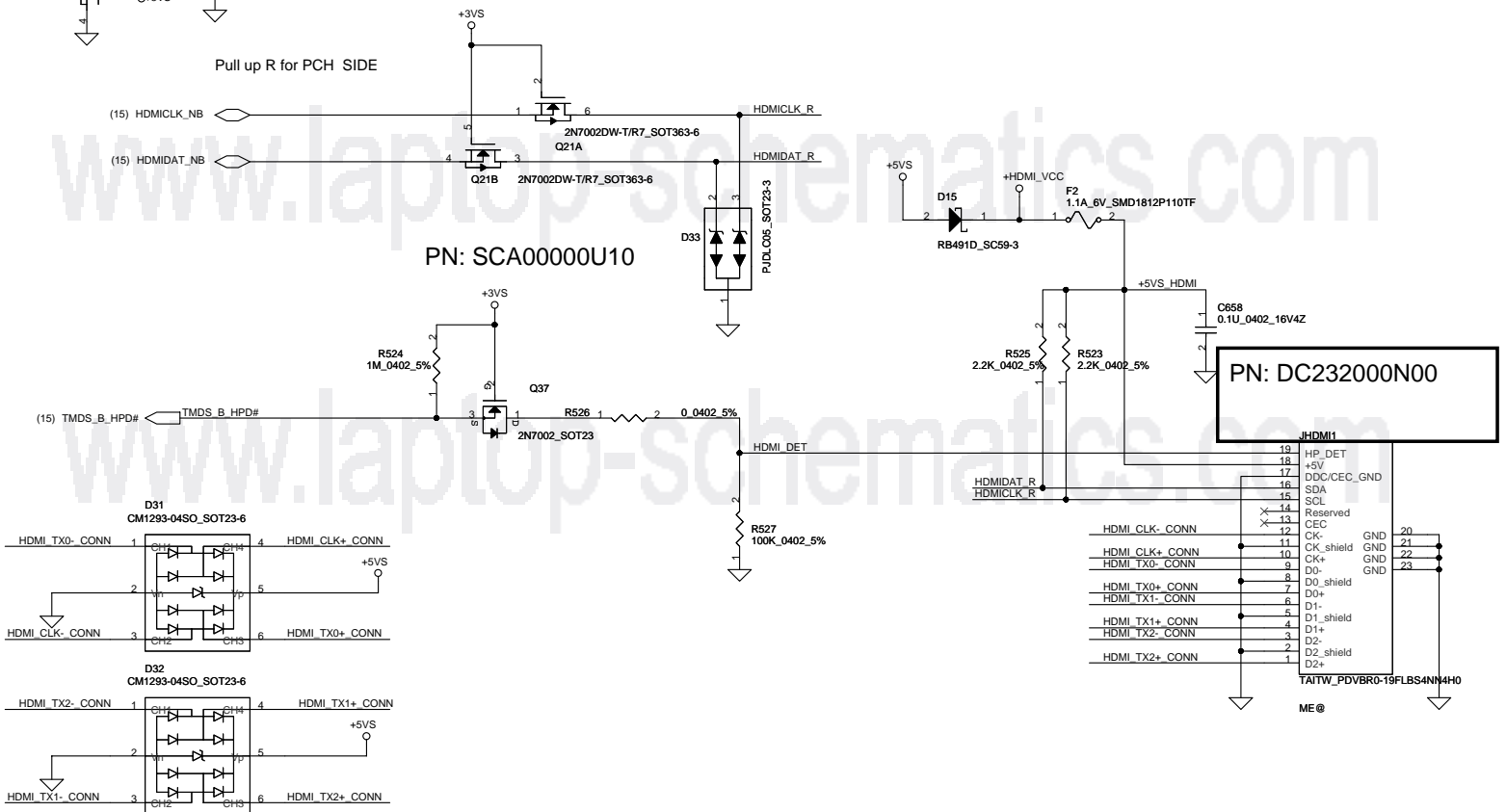
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(15) HDMI_CLK+_CK	HDMI_CLK+_CK	R508	1	2	0.0402_5%	HDMI_CLK+_CONN
(15) HDMI_CLK-_CK	HDMI_CLK-_CK	R509	1	2	0.0402_5%	HDMI_CLK-_CONN
(15) HDMI_TX0+_CK	HDMI_TX0+_CK	R510	1	2	0.0402_5%	HDMI_TX0+_CONN
(15) HDMI_TX0-_CK	HDMI_TX0-_CK	R511	1	2	0.0402_5%	HDMI_TX0-_CONN
(15) HDMI_TX1+_CK	HDMI_TX1+_CK	R512	1	2	0.0402_5%	HDMI_TX1+_CONN
(15) HDMI_TX1-_CK	HDMI_TX1-_CK	R513	1	2	0.0402_5%	HDMI_TX1-_CONN
(15) HDMI_TX2+_CK	HDMI_TX2+_CK	R514	1	2	0.0402_5%	HDMI_TX2+_CONN
(15) HDMI_TX2-_CK	HDMI_TX2-_CK	R515	1	2	0.0402_5%	HDMI_TX2-_CONN



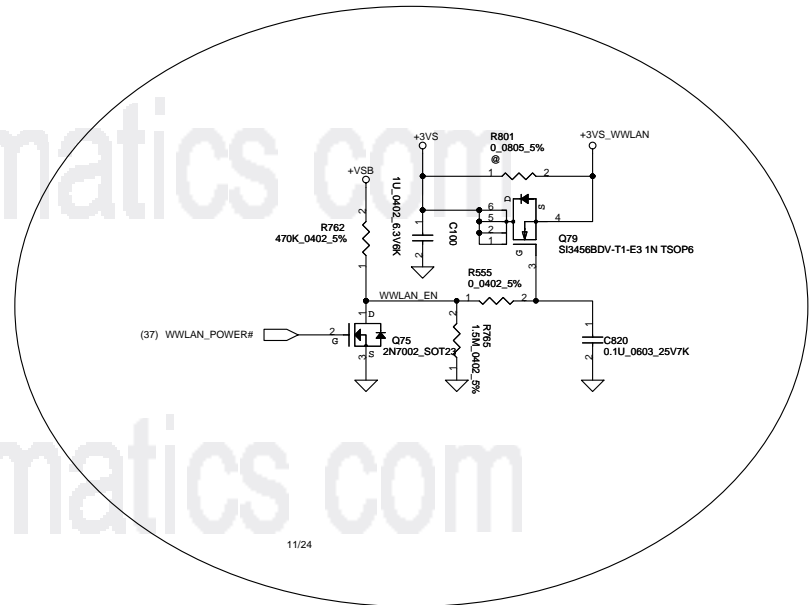
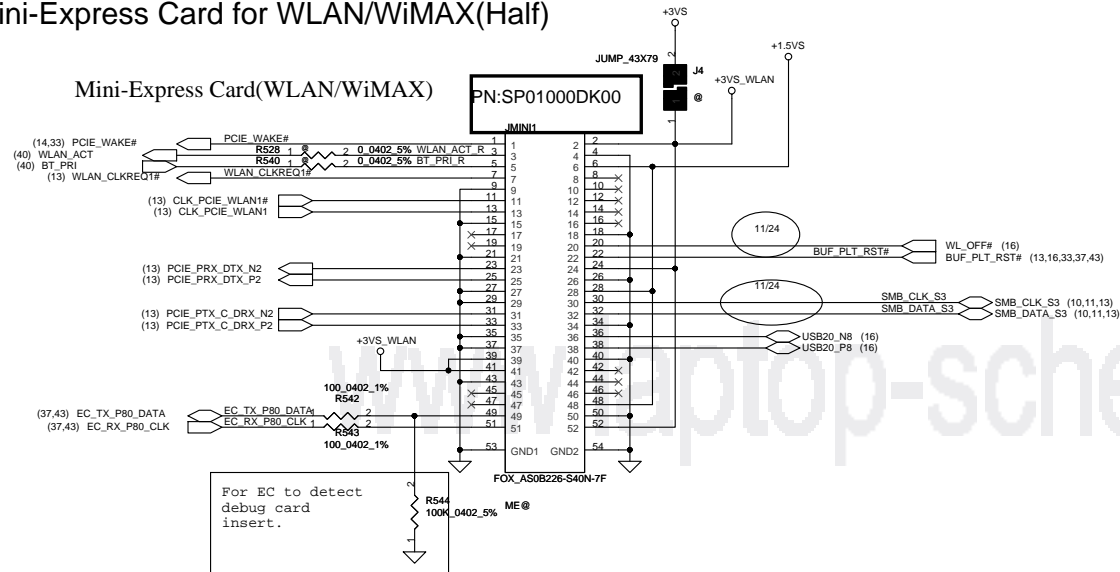
Pull up R for PCH SIDE



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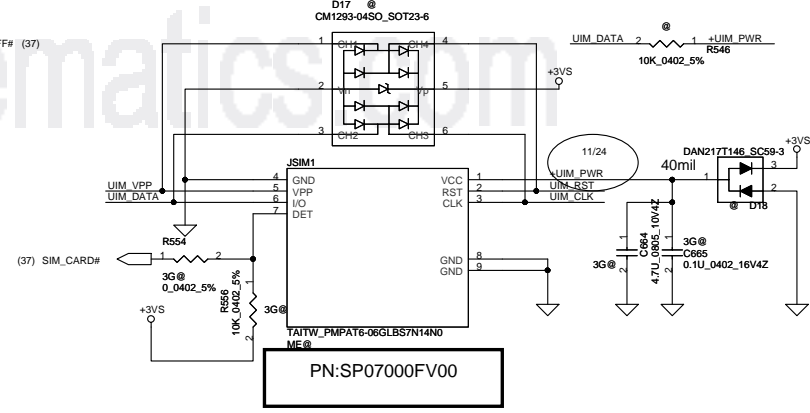
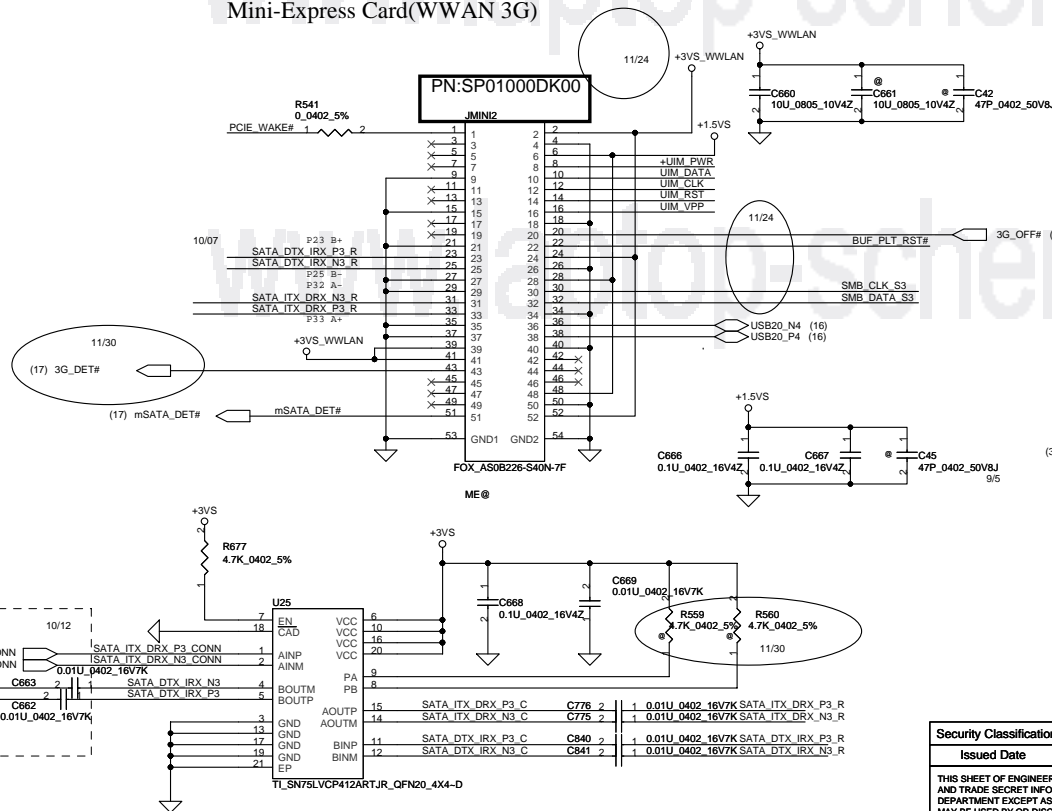
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Mini-Express Card for WLAN/WiMAX(Half)

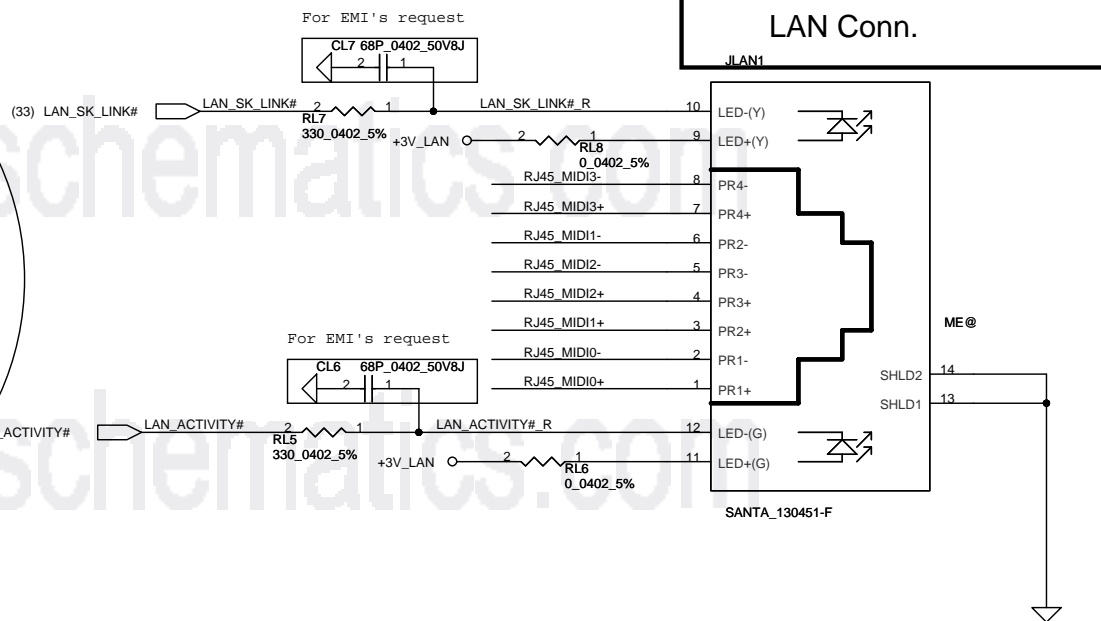
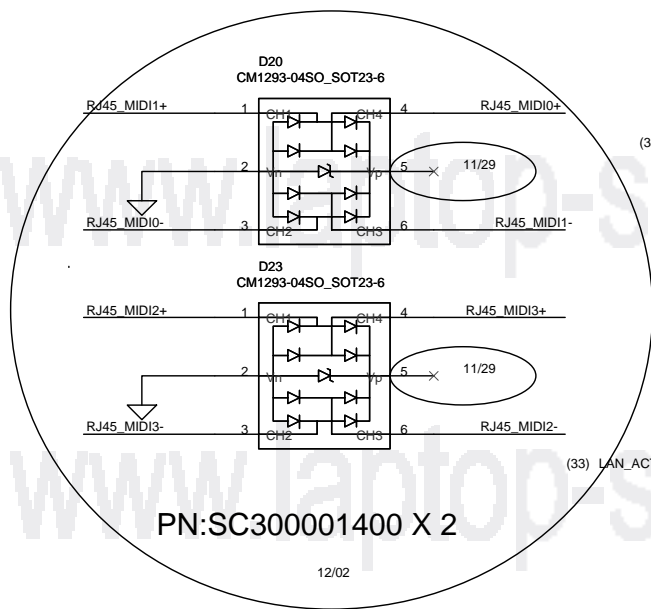
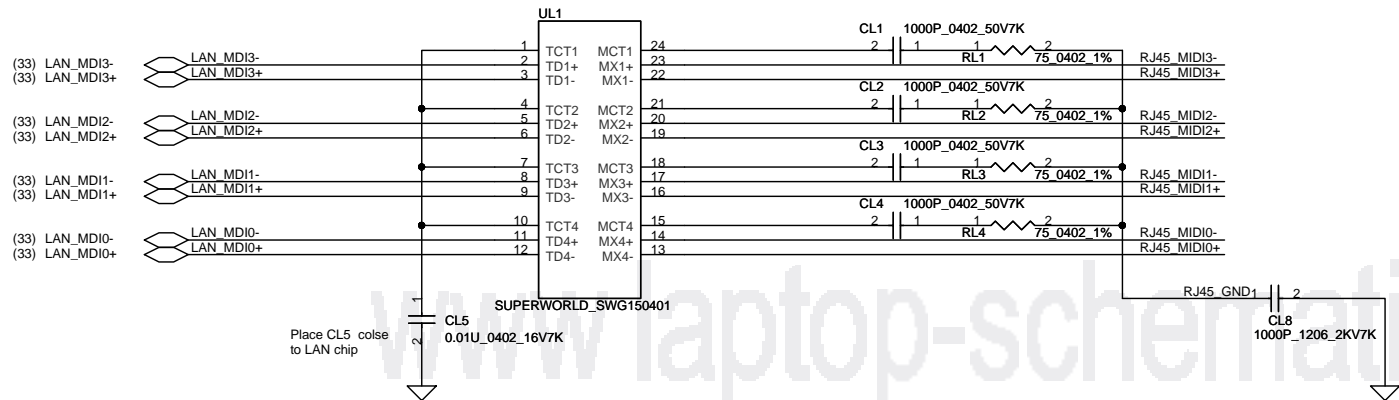


Mini-Express Card for WWAN/mSATA(Full)

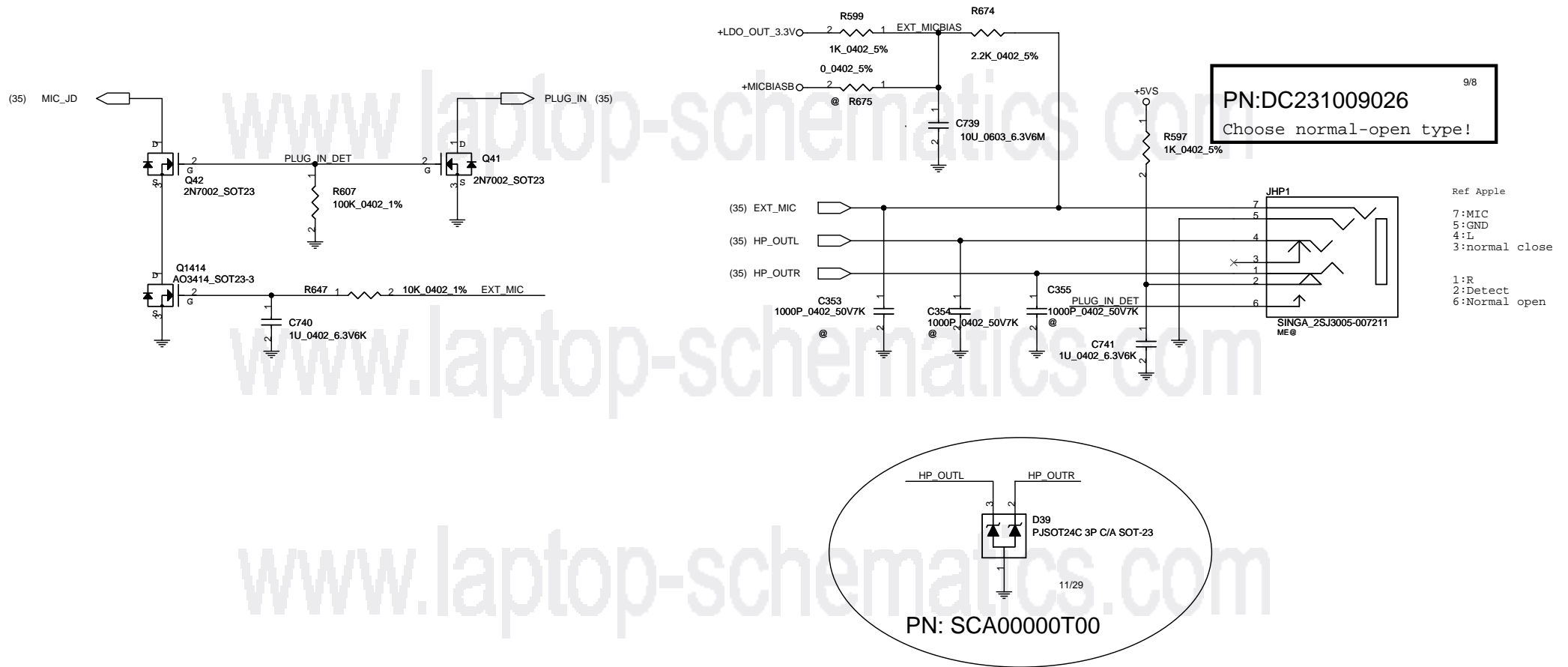
Mini-Express Card(WWAN 3G)



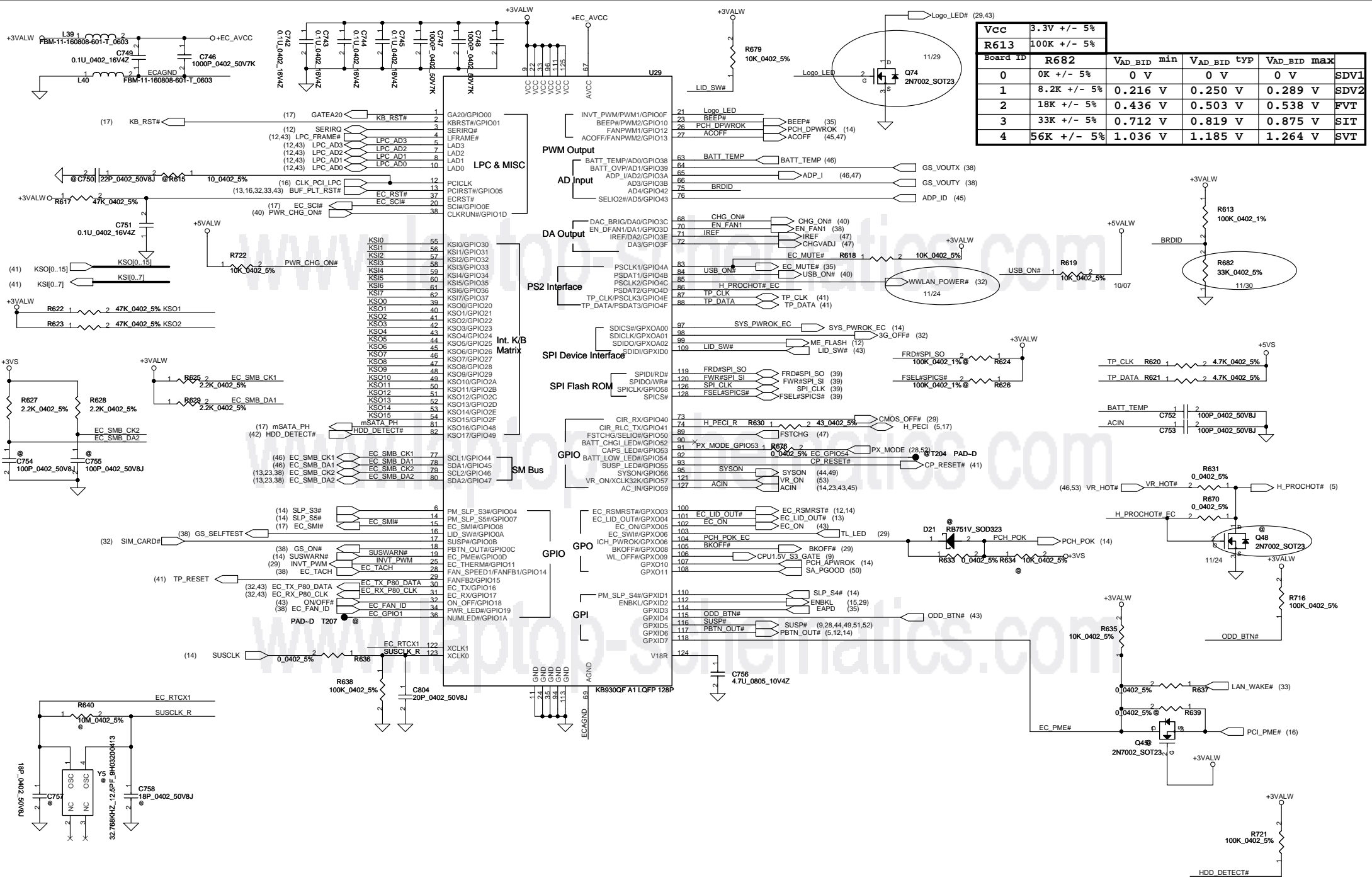
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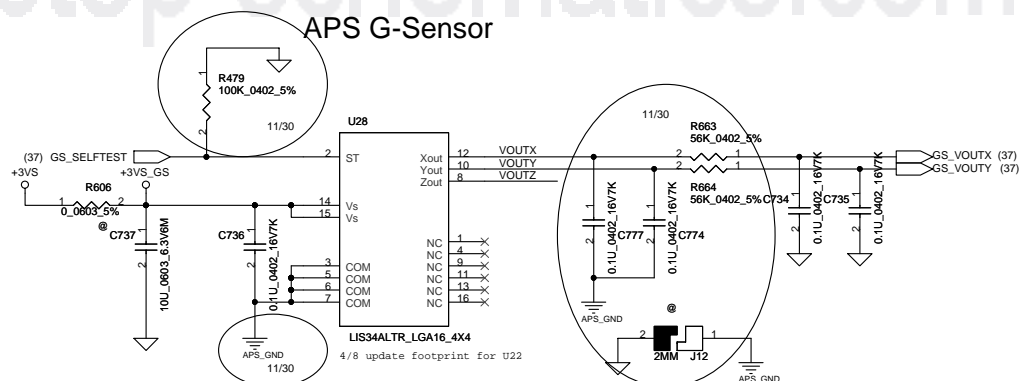
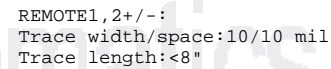
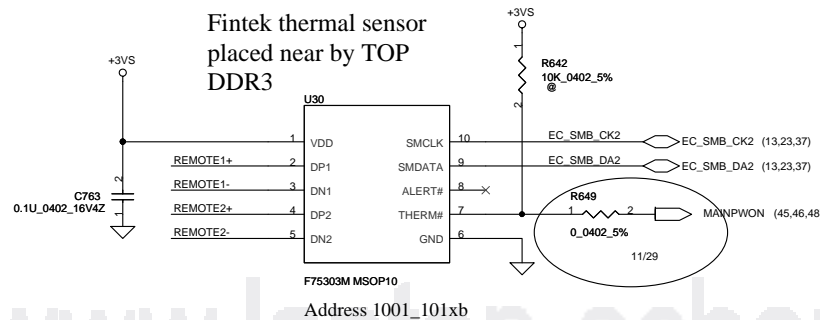


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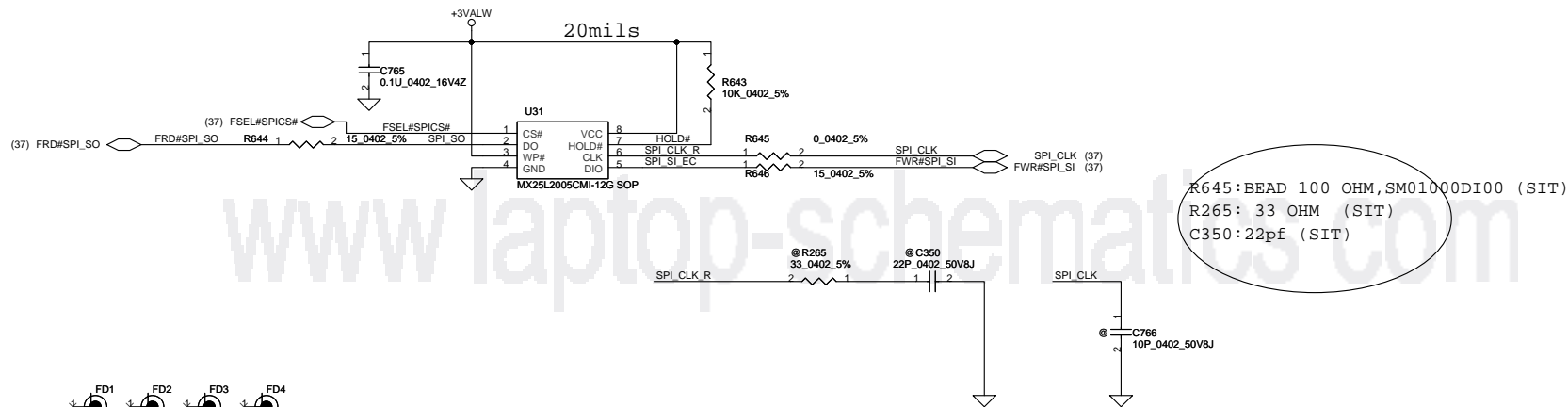
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FOR EC 128KB SPI ROM
(150mil PACKAGE)
PN:SA00002C100

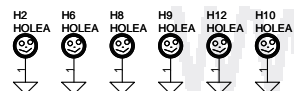


R645: BEAD 100 OHM, SM01000DI00 (SIT)
R265: 33 OHM (SIT)
C350: 22pf (SIT)



E TYPE H_2.5

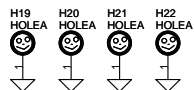
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F TYPE H_2P3



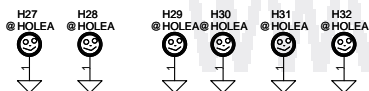
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G TYPE H_3.8P8



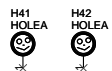
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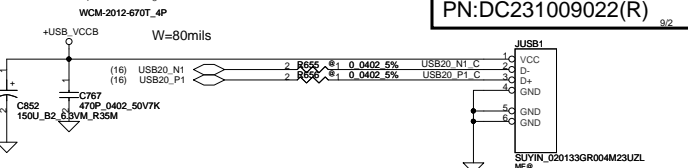
H TYPE H_2.3



D TYPE H_2P8x4P8N



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[illegible]

U33

APL3510BK1_S08

Low Active

C768 0.1U_0402_16V4Z

(37)

USB_ON# (4)

GND

IN

IN

EN

OUT

OUT

OUT

OC#

+5V_ALW

+USB_VCC

E-SATA COMBO
RIGHT USB
PORT

USB_OC# (16)

C769

1000P_0402_50V7K

+USB_VCC

D25
CM1293-04SO_SOT23-6

+USB_VCCC 1 4 USB20_N0_C +5VALW

2 5

3 6 USB20_P0_C ESATA_DET#

PN: SC300001G00

C821
150P_0402_50VJ
12/2

[illegible]

The schematic diagram illustrates the USB_OC# driver circuit. It features a +5VALW supply connected to a 0.1uF capacitor (C843) and the IN pin of a 16V4Z Schmitt trigger (U40). The output of U40 is connected to the IN pin of an APL3510BK1 S08 Low Active MOSFET (U40). The MOSFET's source is connected to GND, and its drain is connected to the USB_OC# pin (16). A +5V_CHGUSB supply is connected to the OUT pin of U40 and the GND pin of the MOSFET. A 1000pF capacitor (C844) is connected between the USB_OC# pin and GND.

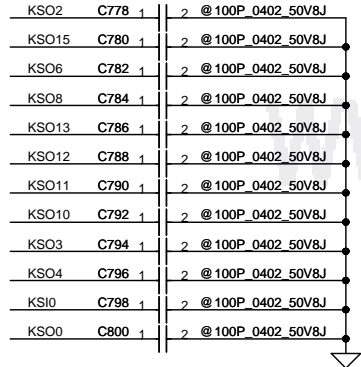
Figure 10: USB2.0 PHY connection diagram. The diagram shows a USB2.0 PHY block with pins PW/SRST_EN# (1), USB2_0_N#_C (2), USB2_0_P#_G (3), DM (4), and DND (5). These pins are connected to a MAX14566E1A_TDFNEP8_2X2-D. The PHY also has pins CB (6), TDM (7), TDP (8), and VCC (9). These are connected to a USB2.0 block with pins CHG_ON# (10), USB2_0_N# (16), USB2_0_P# (16), and S5VALW (16). The USB2.0 block is connected to a CHG_ON# (3) pin. The PHY also has a pin R609 connected to a 100K_0402_5% resistor, which is connected to a C842 capacitor (0.1U_0402_16V4Z) and a ground symbol.

L43
WCM-2012-670T_4P

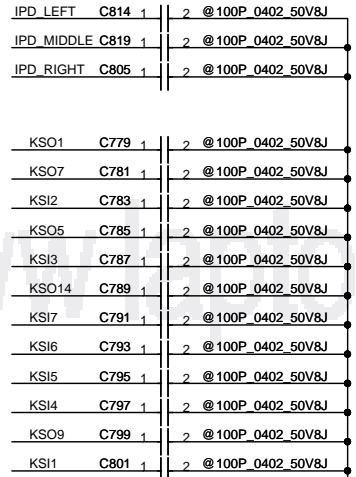
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INT_KBD Conn.

KSII[0..7] KSII[0..7] (37)
KSO[0..15] KSO[0..15] (37)



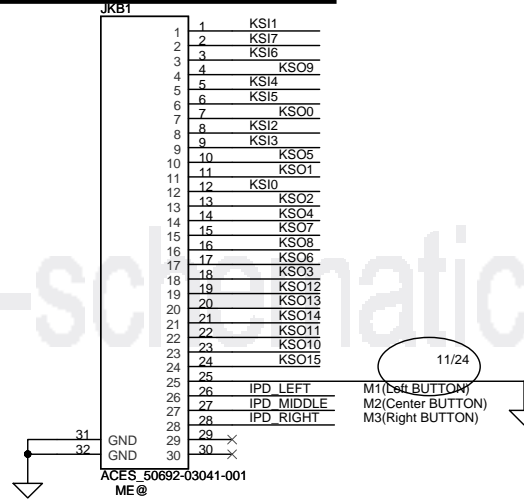
CONN PIN define need double check



Reserve for ESD.

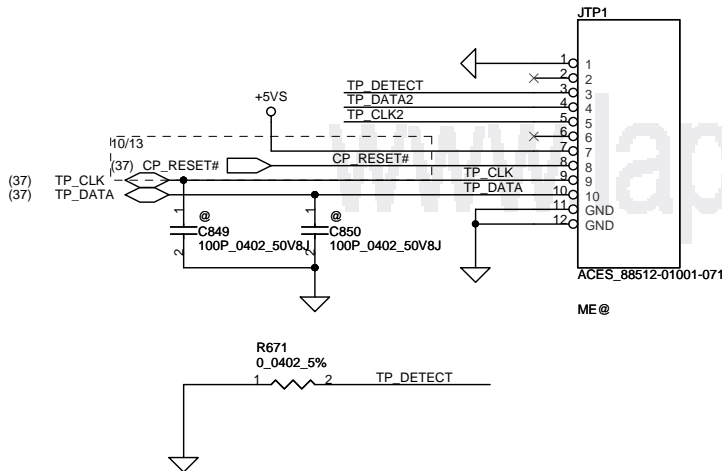
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9/8



PN:LTCX002RM00

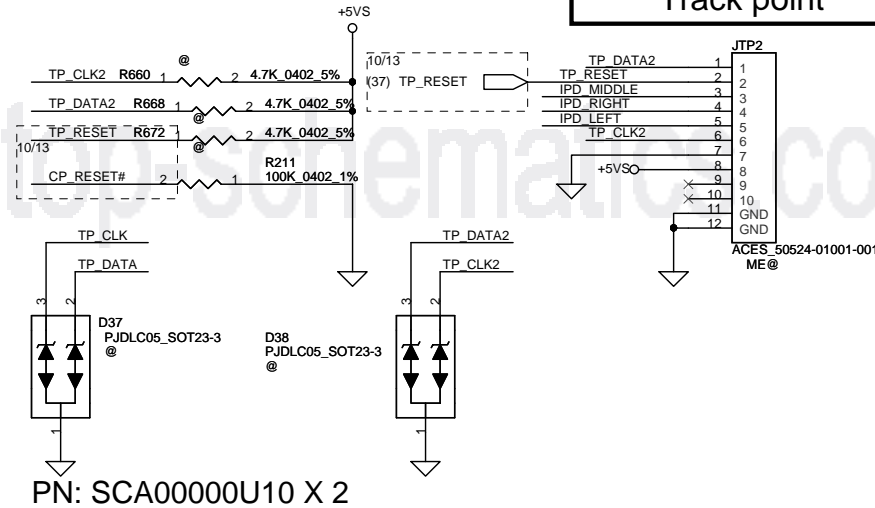
Click pad 10PIN



PN:SP011009011

Track point

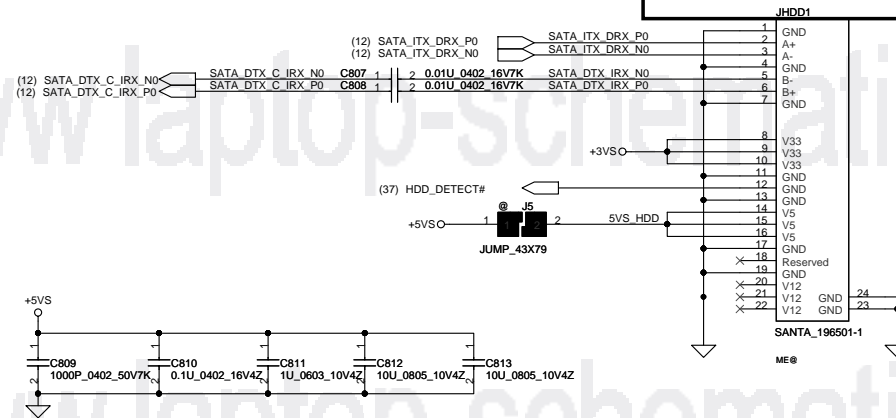
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PN: SCA00000U10 X 2

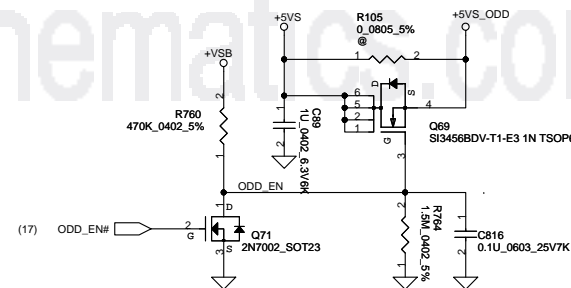
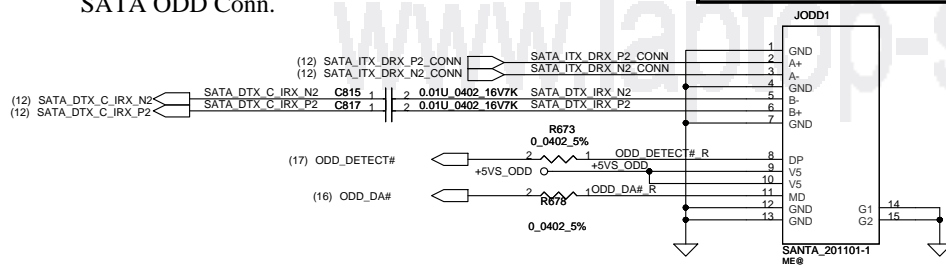
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PN:DC011009021(R)
SATA HDD Conn.

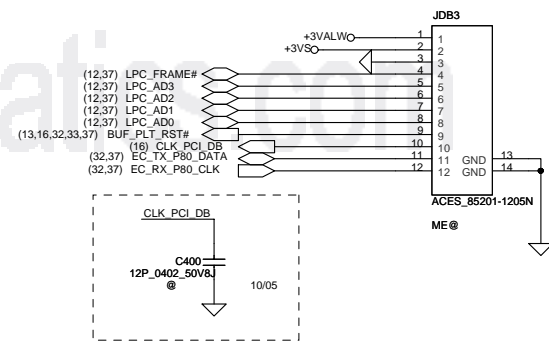
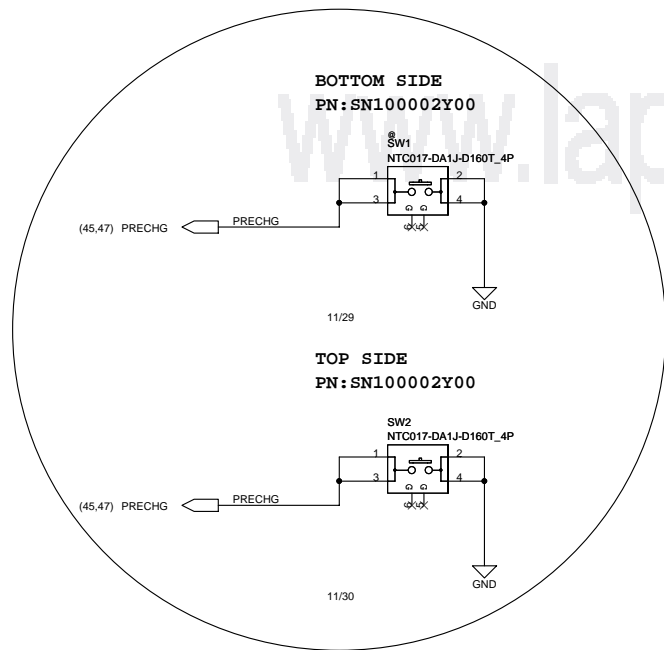
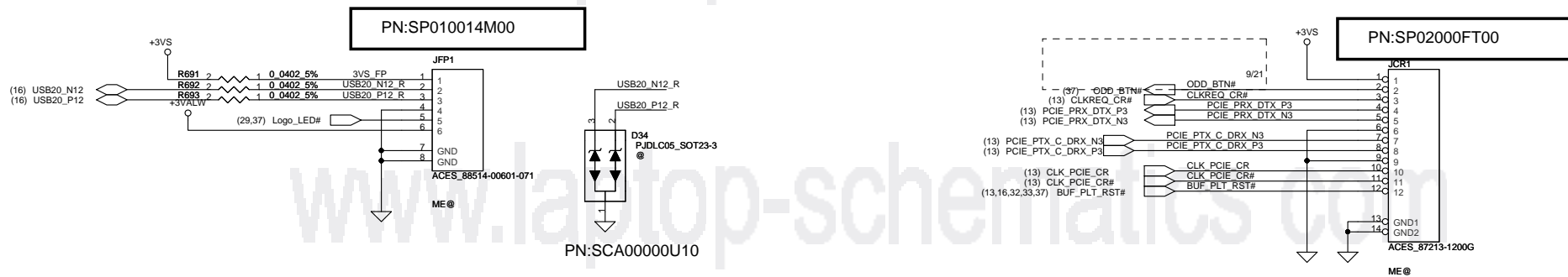
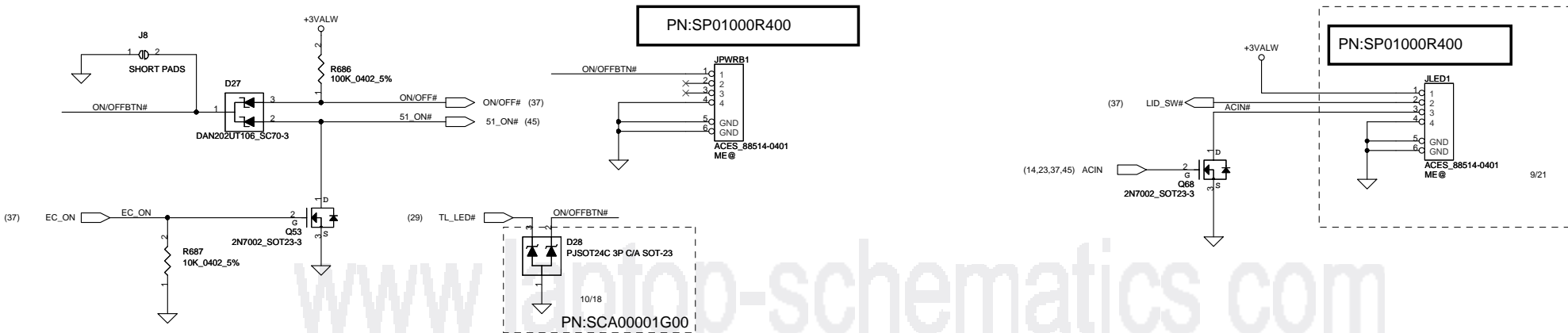


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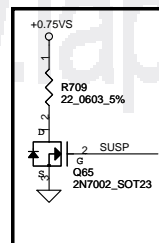
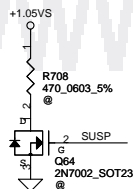
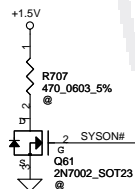
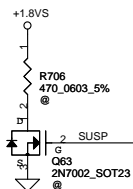
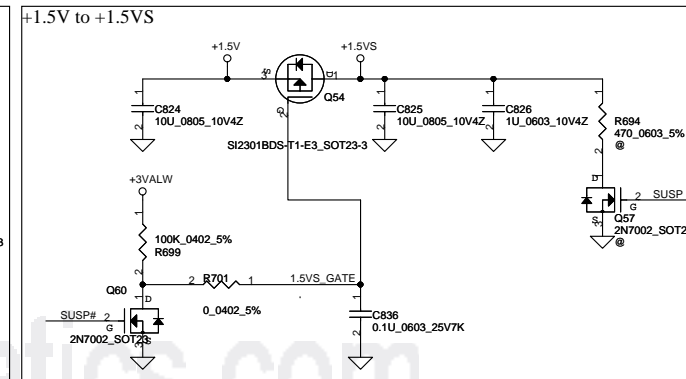
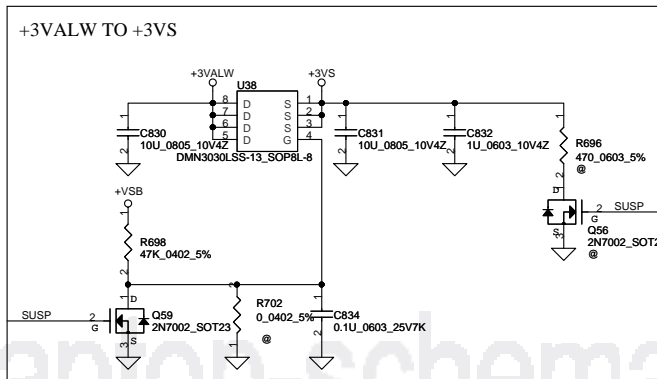
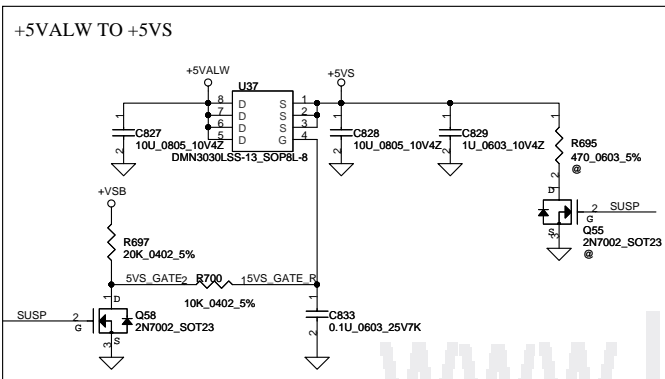
SATA ODD Conn.



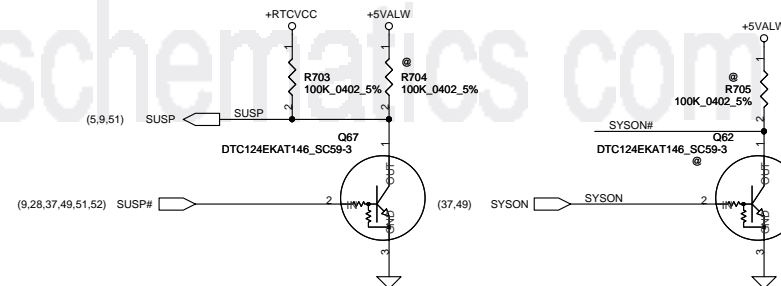
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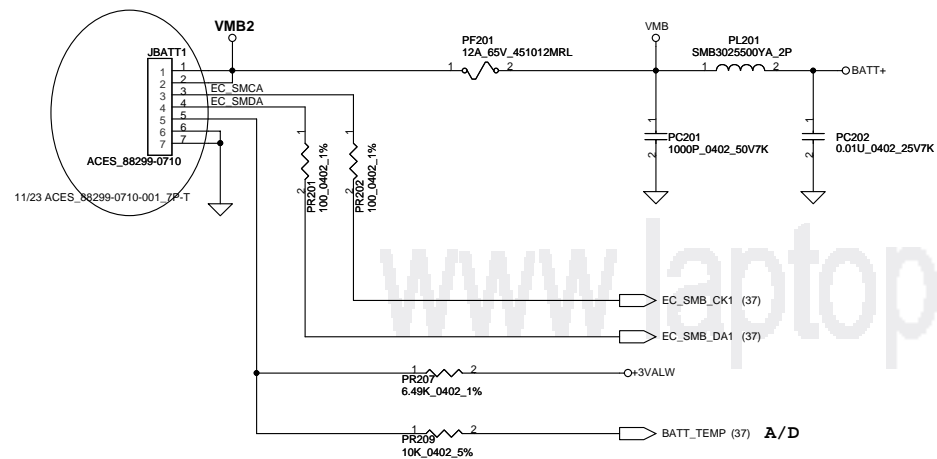
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										4019A1
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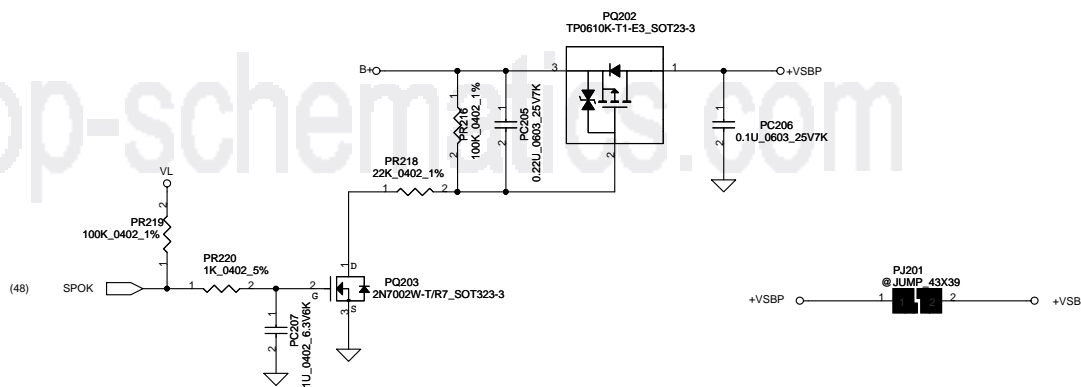
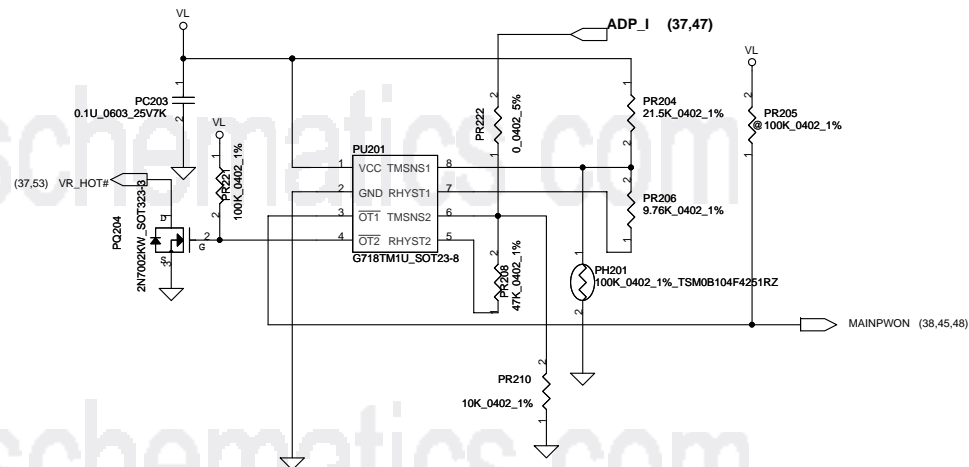
For Intel S3 Power Reduction.



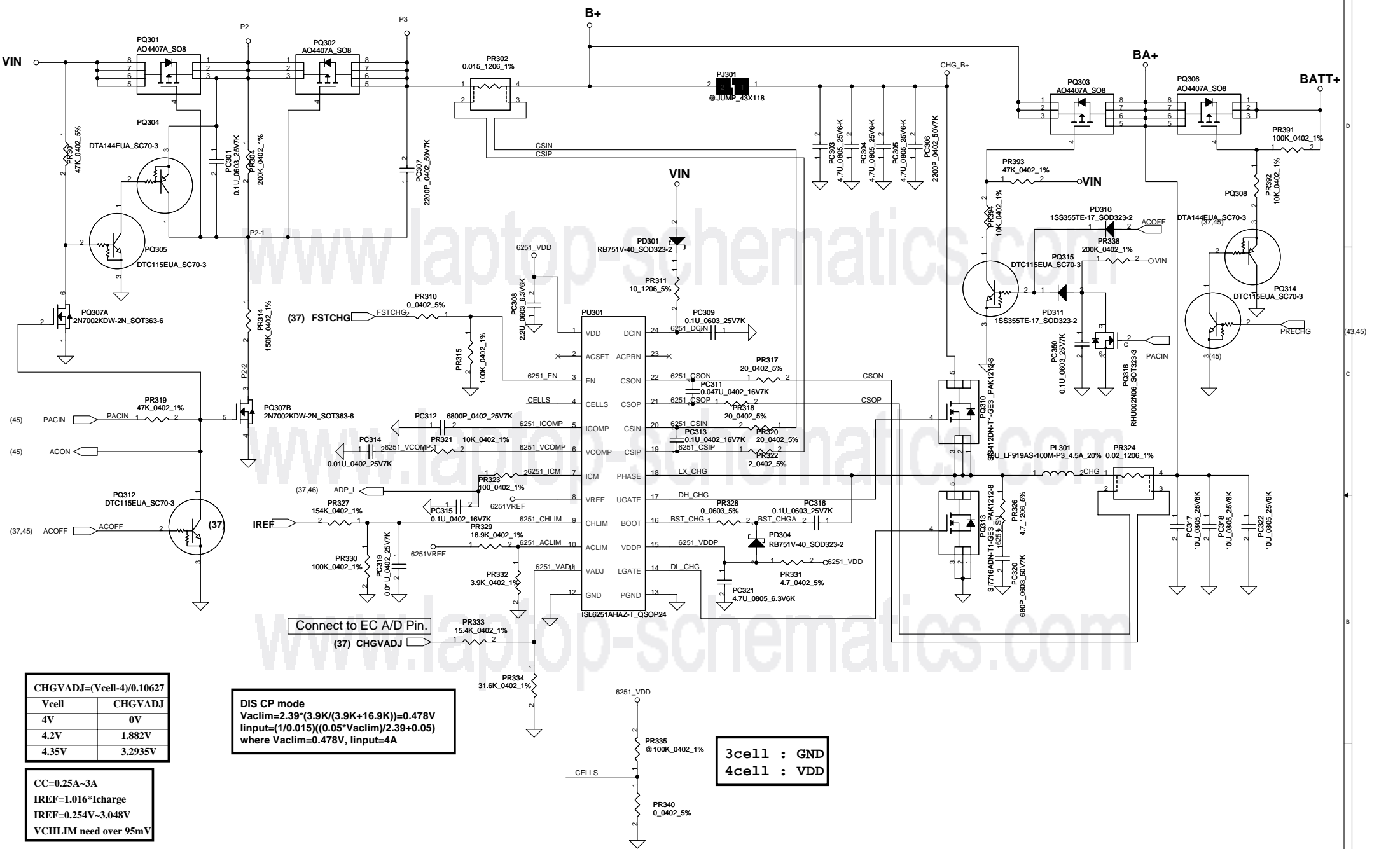
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PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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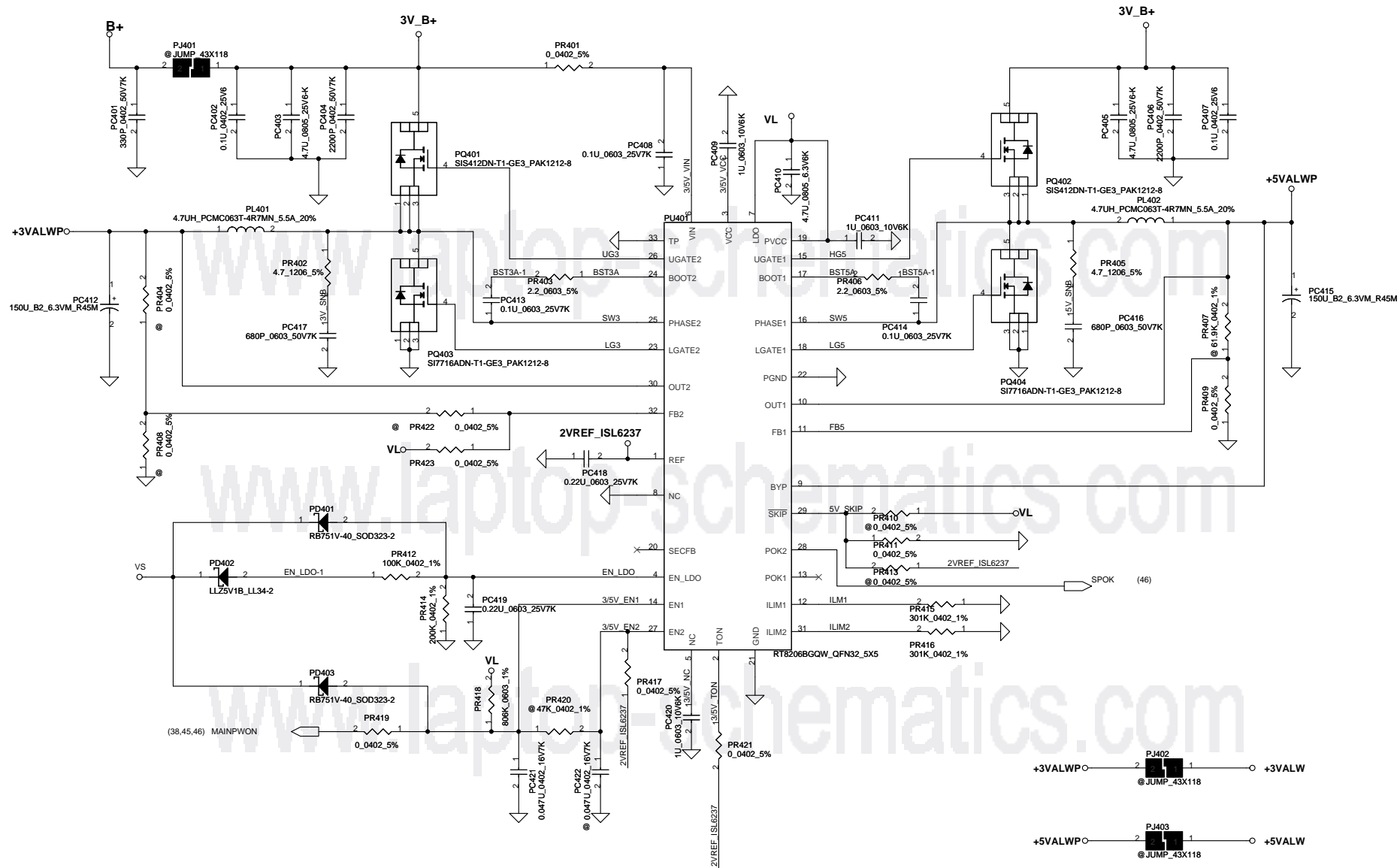


CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

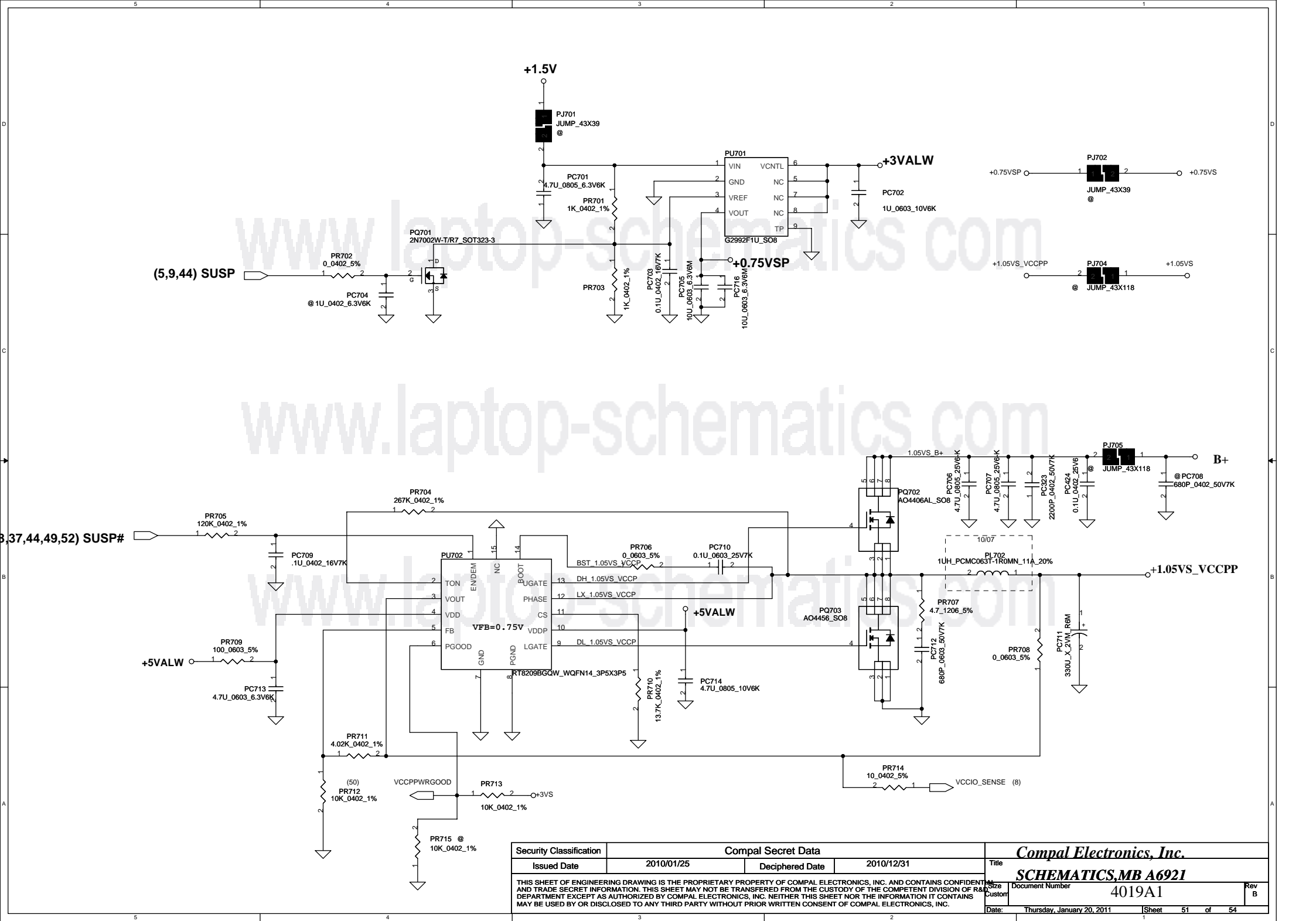
CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

DIS CP mode
 $V_{acim}=2.39*(3.9K/(3.9K+16.9K))=0.478V$
 $I_{inpu}=(1/0.015)/((0.05*V_{acim})/2.39+0.05)$
where $V_{acim}=0.478V$, $I_{inpu}=4A$

3cell : GND
4cell : VDD

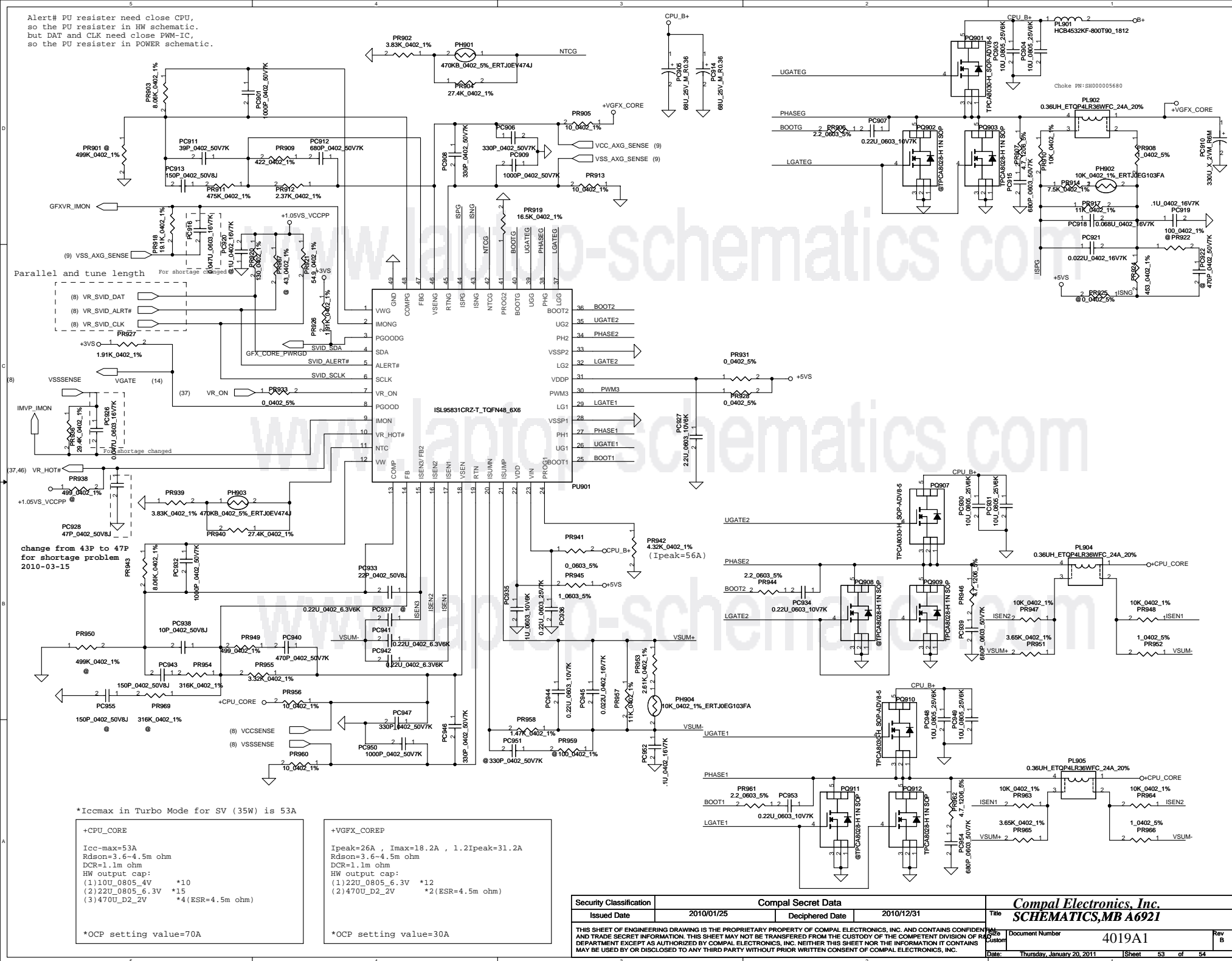


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Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.



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