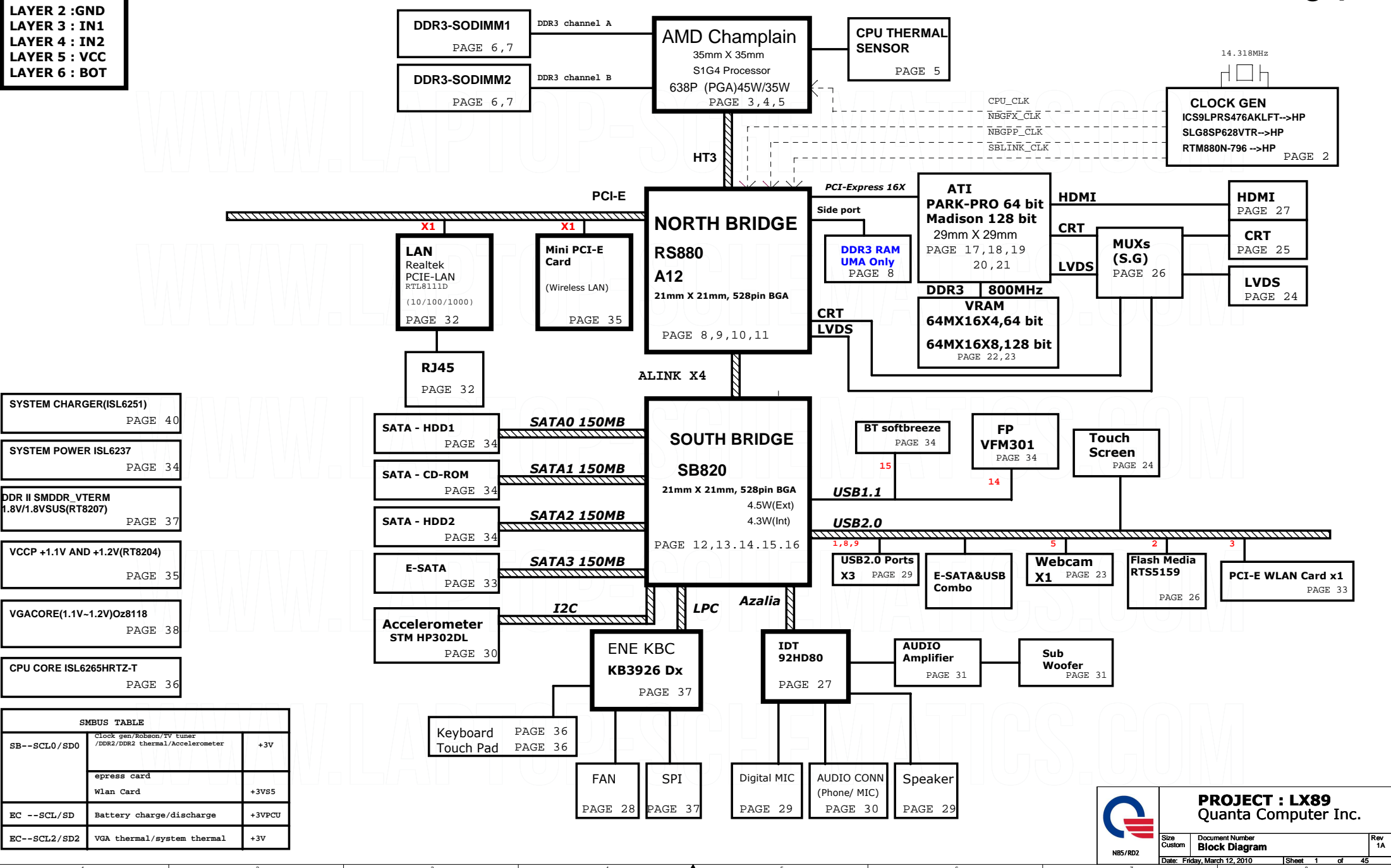




LX89 SYSTEM DIAGRAM

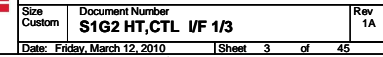
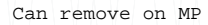
PCB STACK UP

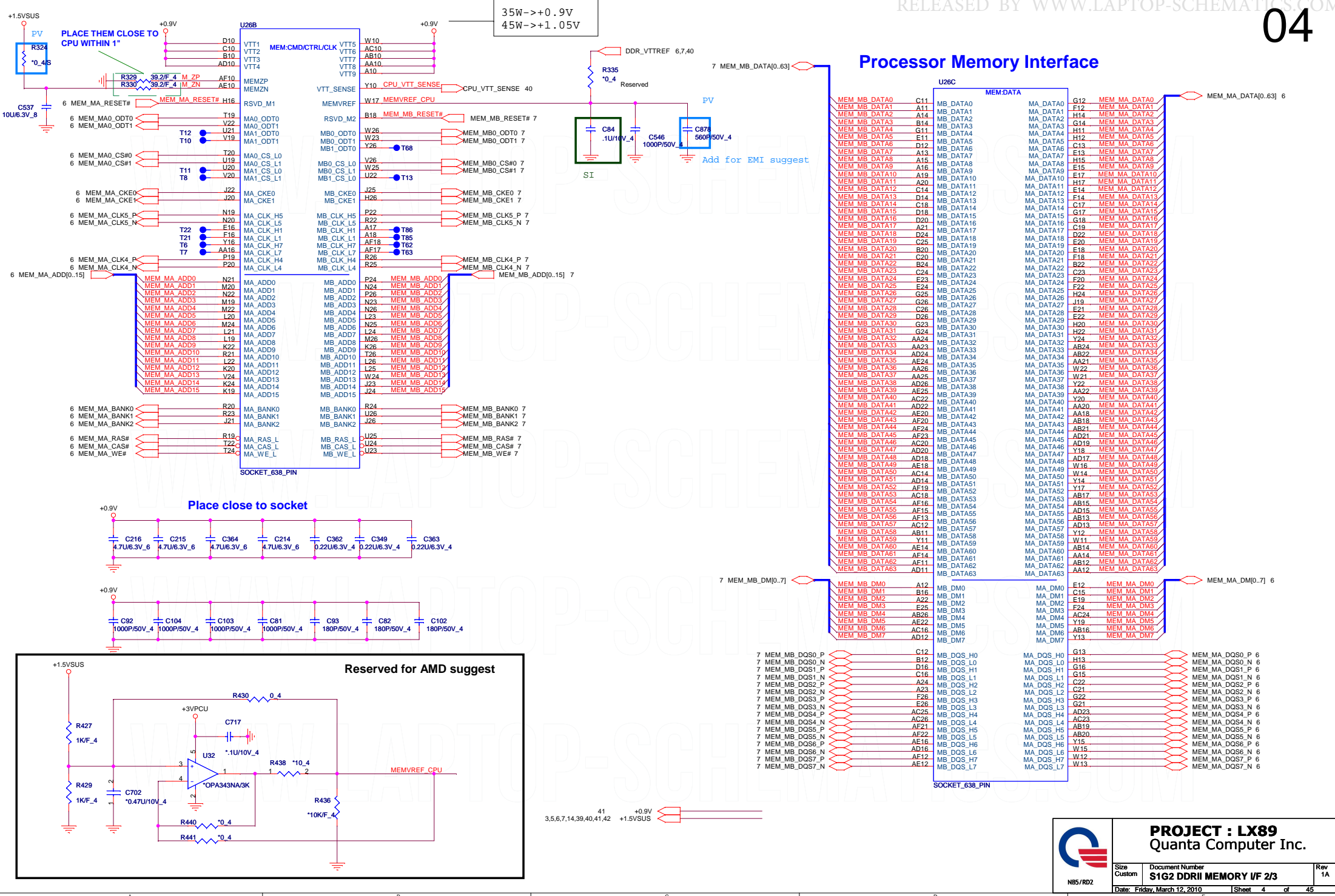
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT




PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Friday, March 12, 2010		Sheet 1 of 45



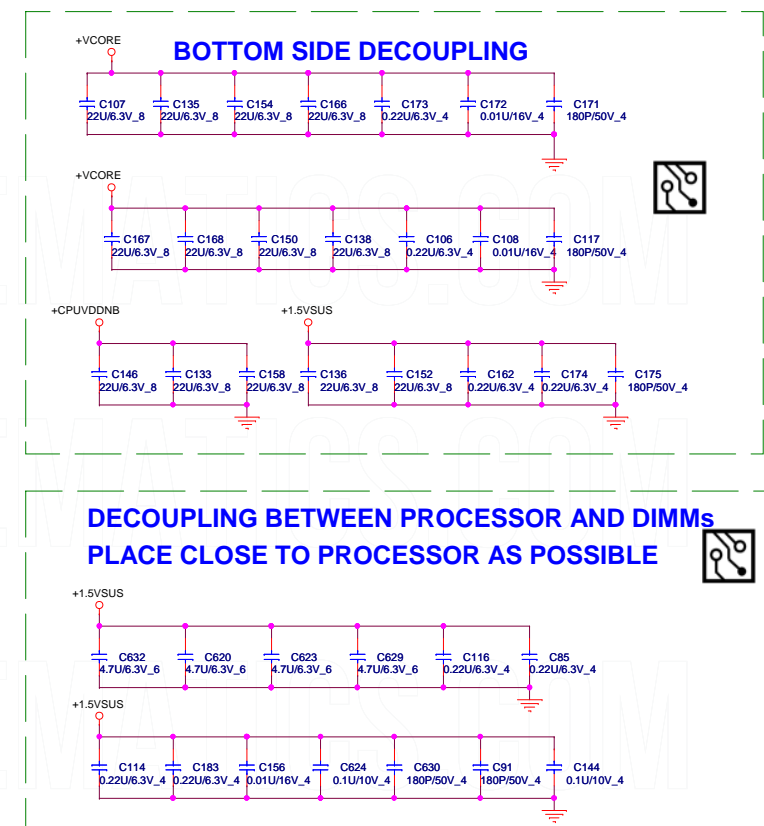




NBS/RD2

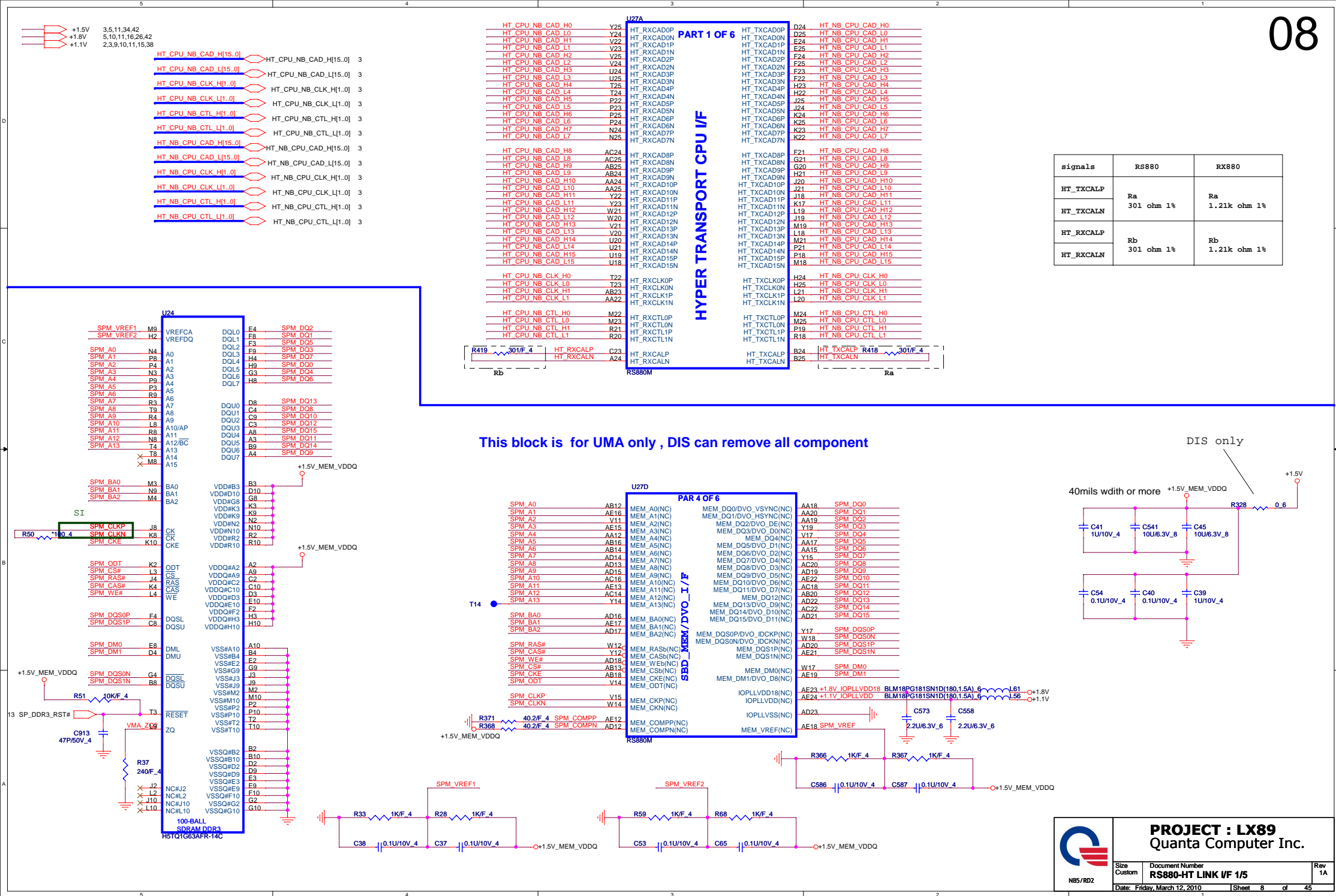
PROJECT : LX89
Quanta Computer Inc.

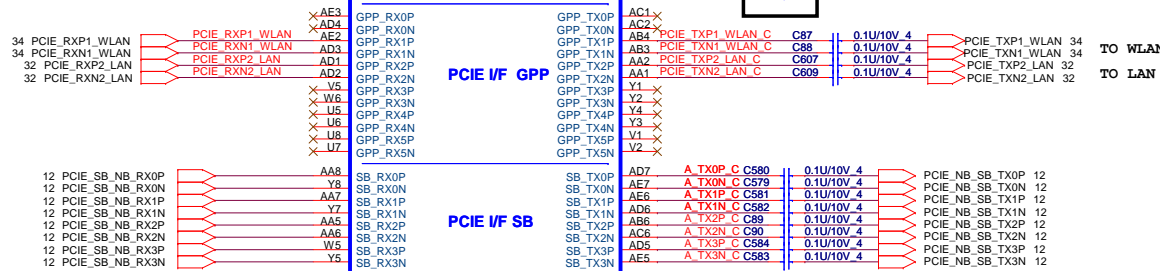
Size Custom	Document Number S1G2 DDRII MEMORY I/F 2/3	Rev 1A
Date: Friday, March 12, 2010		Sheet 4 of 45



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

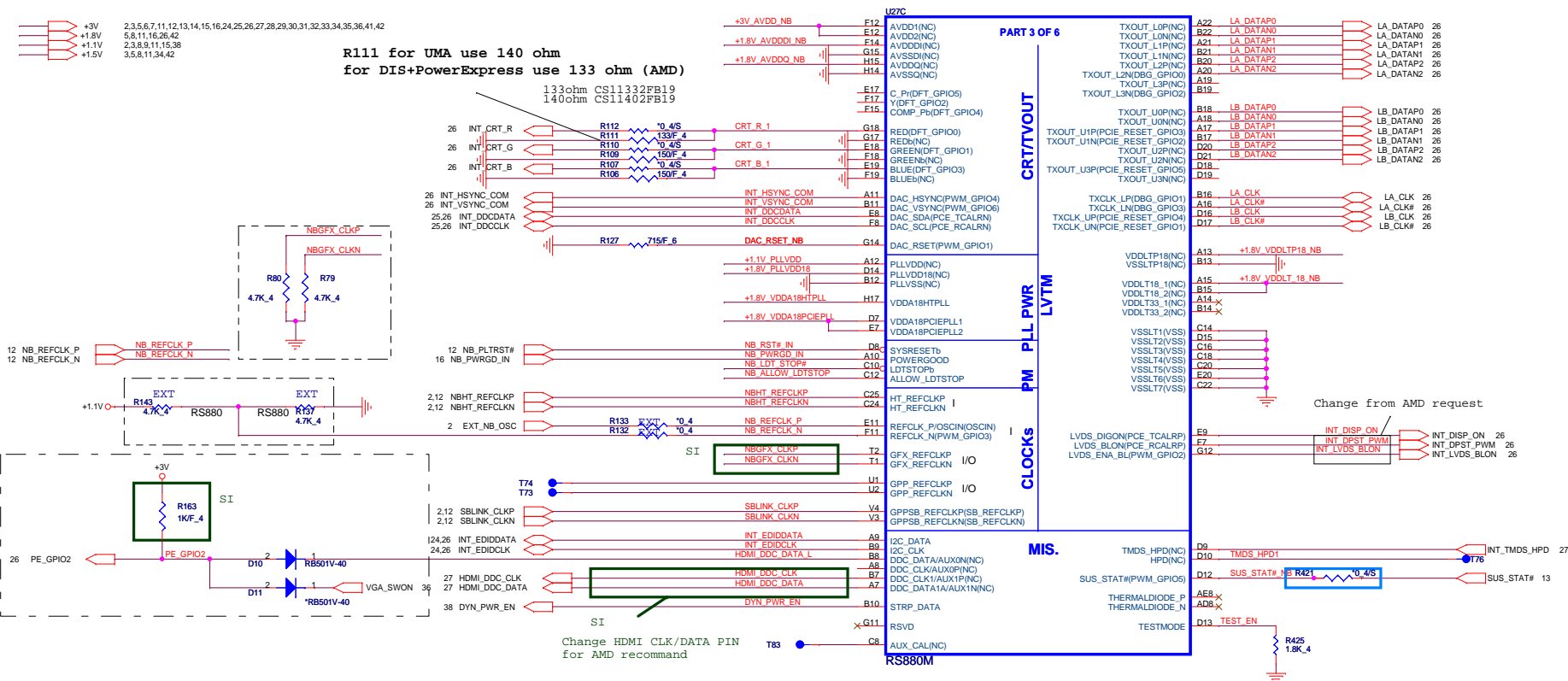




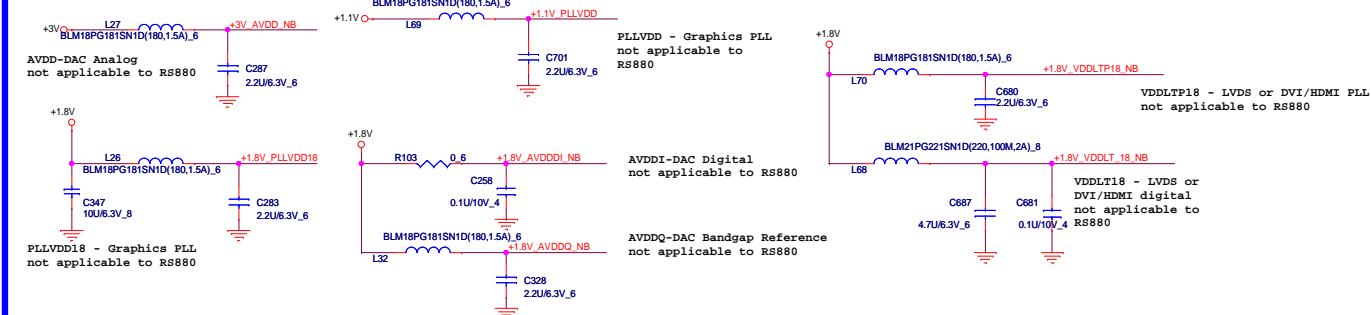
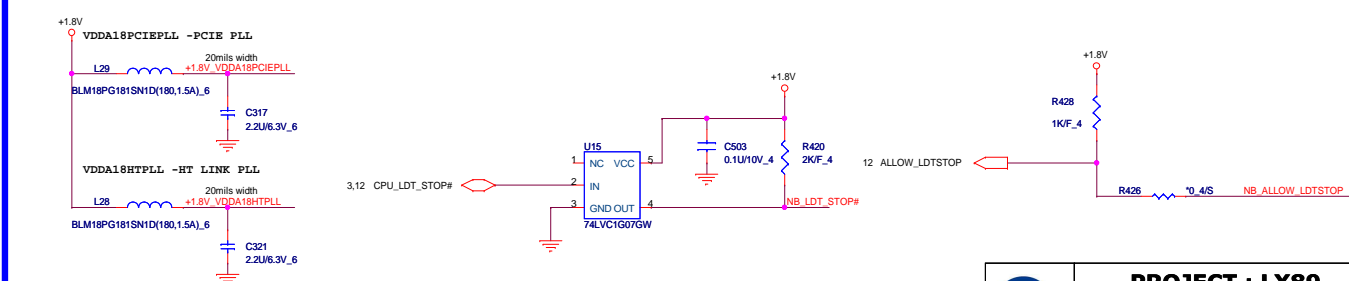


DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

133ohm CS11332FB19
140ohm CS11402FB19



RS880M --- ADD

[illegible]

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable



RS880M: Enables Side port memory

RS880M:INT_HSYNC_COM

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available

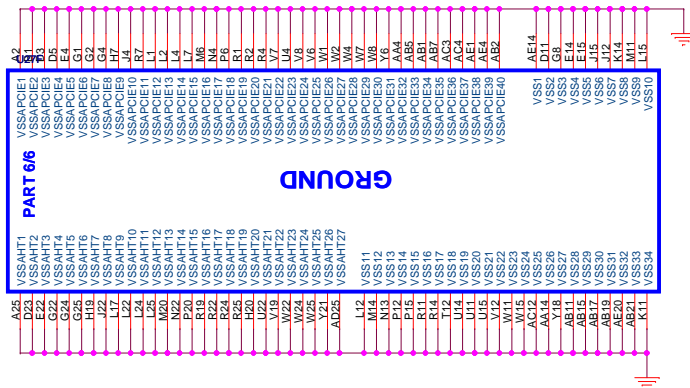
0 = Memory Side port available

Register Readback of strap: NB CLKCFG:CLK TOP SPARE D[1]



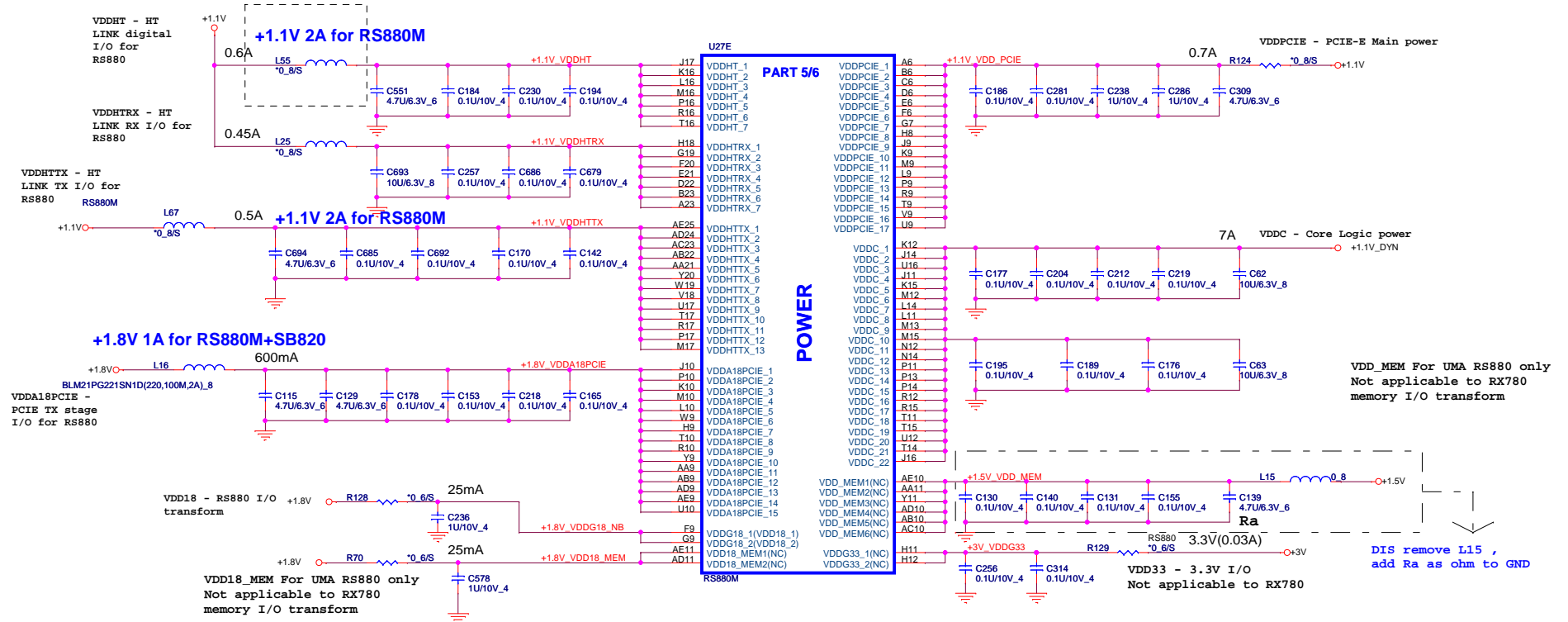
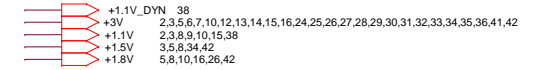
For extrnal EEPROM Debug only

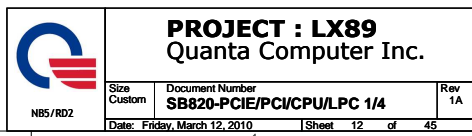
RS880

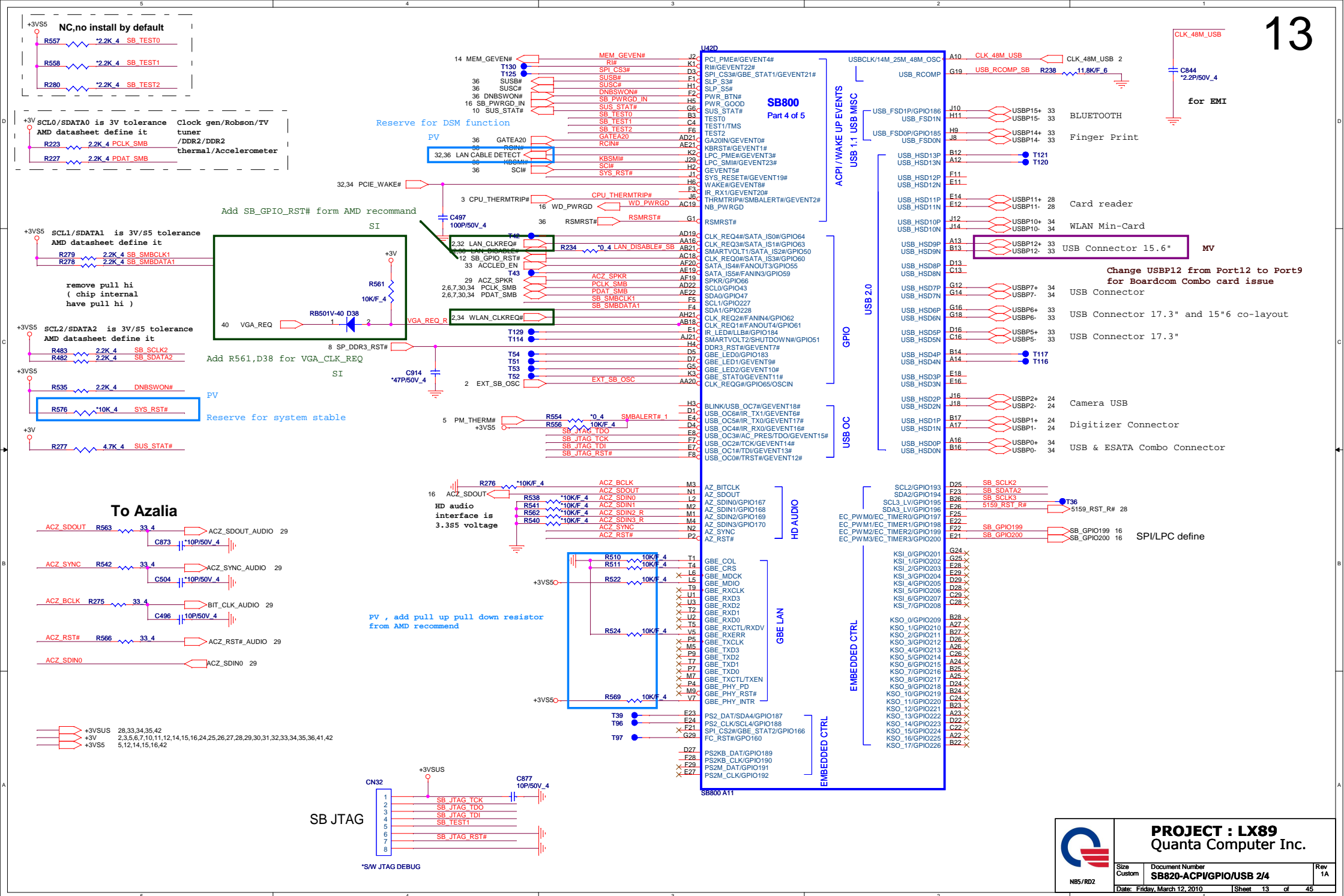


RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLTP18	+1.8V
IOPLLVD18	+1.8V	VDDLTP33	NC







SATA PORT 0,1,2,3
can support AHCI
mode

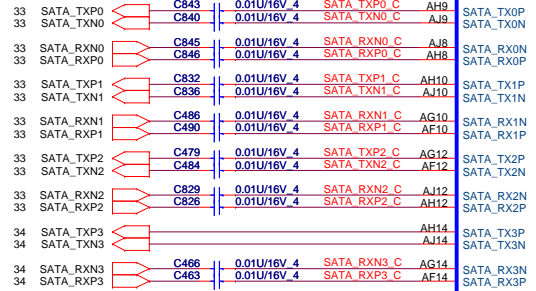
SATA1 HDD

SATA ODD

SATA2 HDD

E-SATA

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820



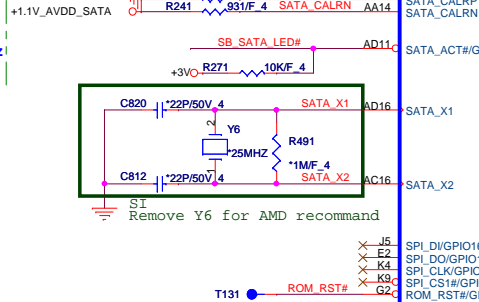
XTLVDD_SATA-- SATA
crystal power

PLVDD_SATA--
SATA PLL
POWER



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL. 4.99K 1% FOR 100MHz
INTERNAL CLOCK



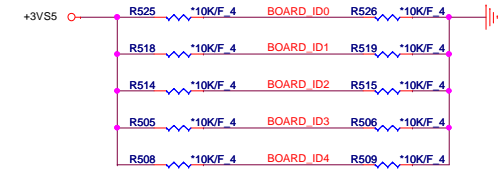
SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/GPIO161

SB800 A11

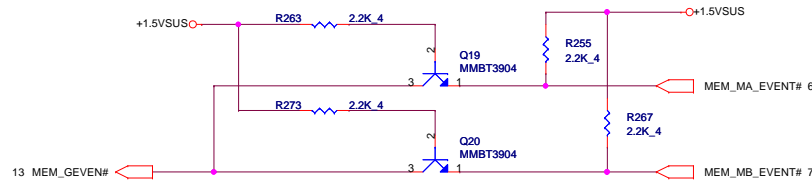
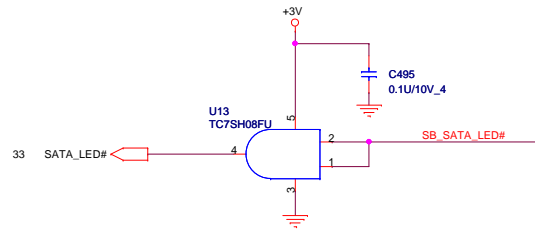
IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

+1.1V_AVDD_SATA 15
+3V 2,3,5,6,7,10,11,12,13,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,41,42
+3VS5 5,12,13,15,16,42

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX9 Madison
0	0	1	0	0	LX8 Park
0	0	1	0	1	LX9 Park
0	0	1	1	0	LX9 Madison(DF)
0	0	1	1	1	LX9 Park(DF)
0	1	0	0	0	LX8 M92
0	1	0	0	1	LX9 M92
0	1	0	1	0	LX9 M92(DF)



VDD-- S/B CORE power

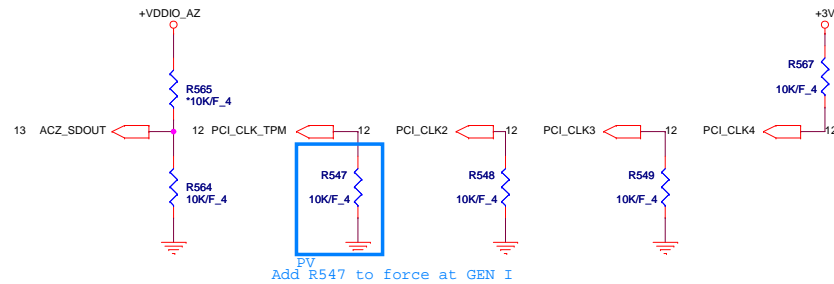


Size Custom	Document Number SB820-PWR/DECOUPLING 4/4	Rev 1A
Date: Friday, March 12, 2010		Sheet 15 of 45



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

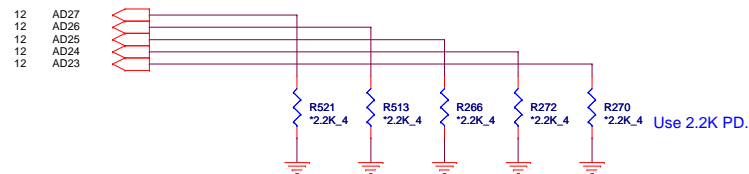


REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

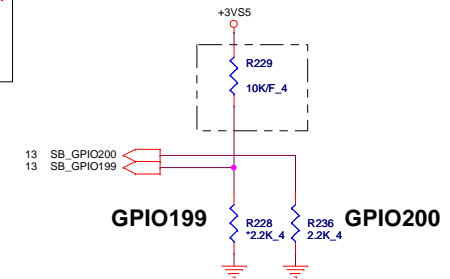


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

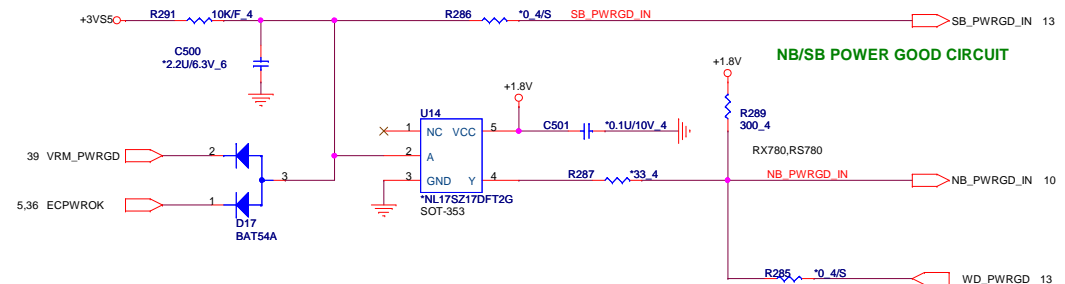
+VDDIO_AZ 5,12,13,14,15,42
+3V 2,3,5,6,7,10,11,12,13,14,15,24,25,26,27,28,29,30,31,32,33,34,35,36,41,42
+3VS5 5,12,13,14,15,42
+1.8V 5,8,10,11,26,42

It must ready
before RSMRST#



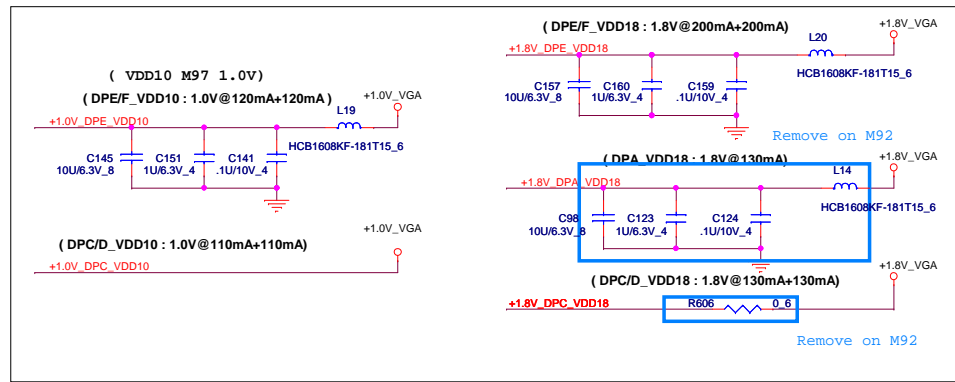
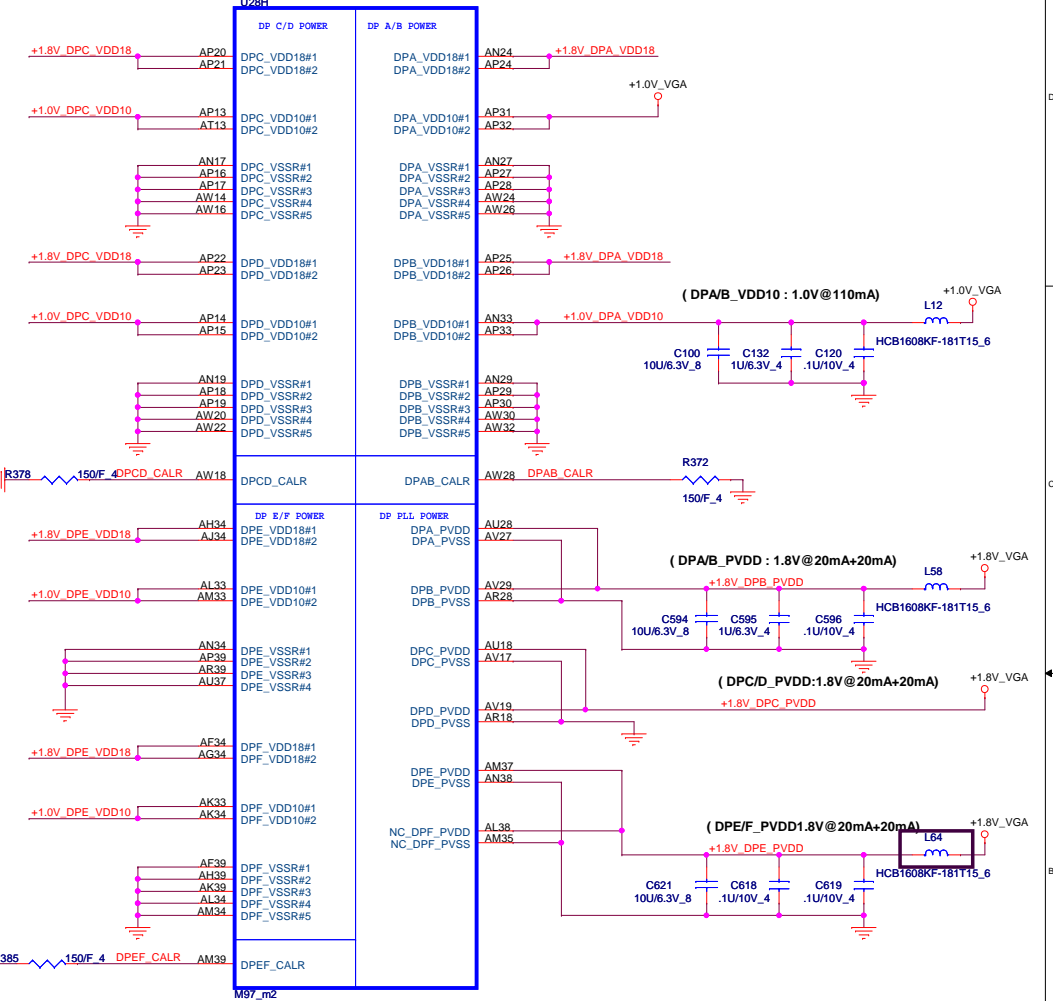
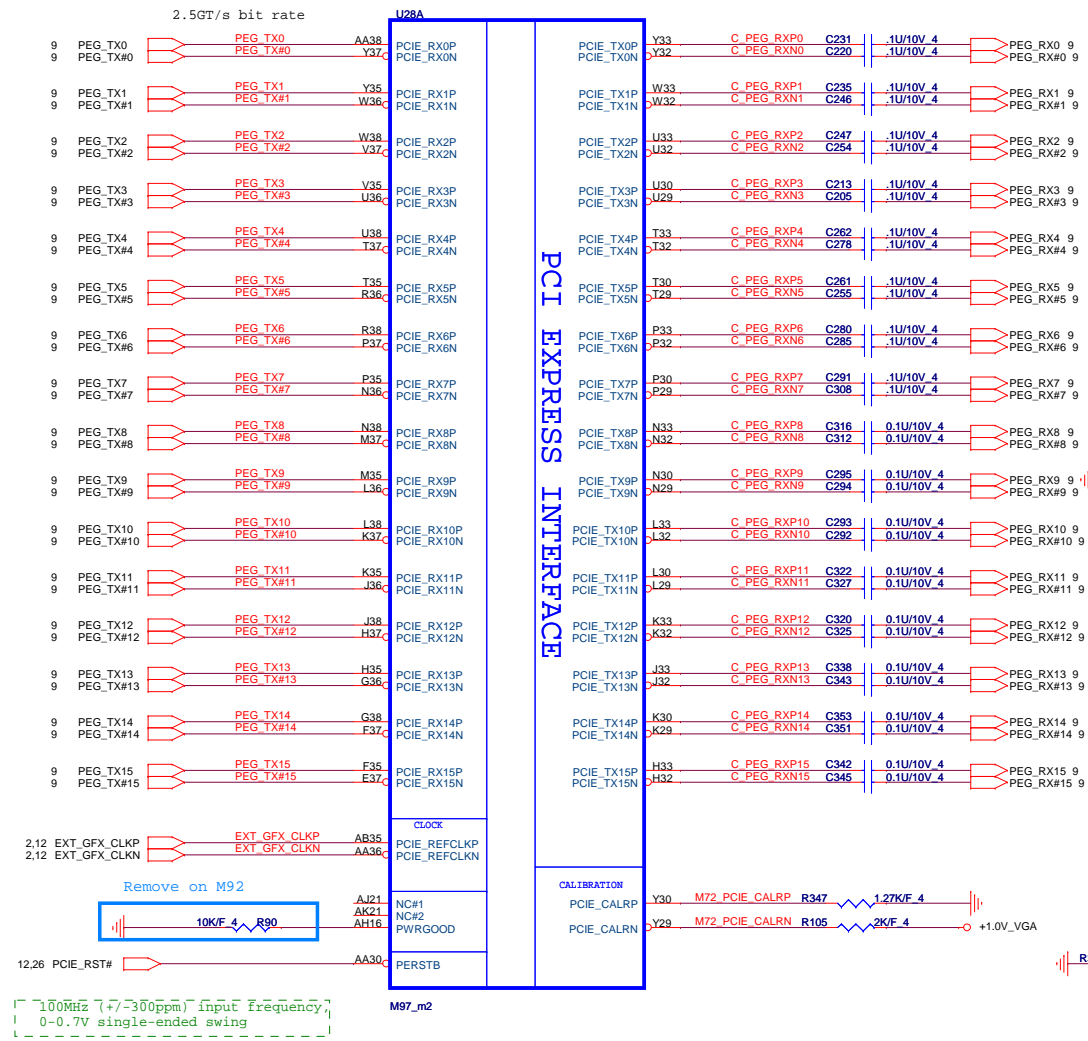
TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

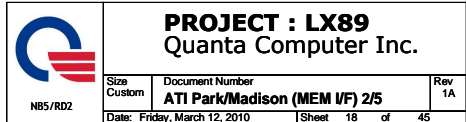
NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number SB820-STRAPS	Rev 1A
	Date: Friday, March 12, 2010	Sheet 16	of 45





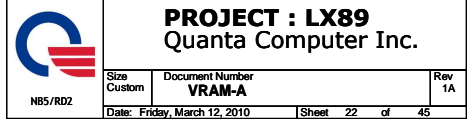


It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.

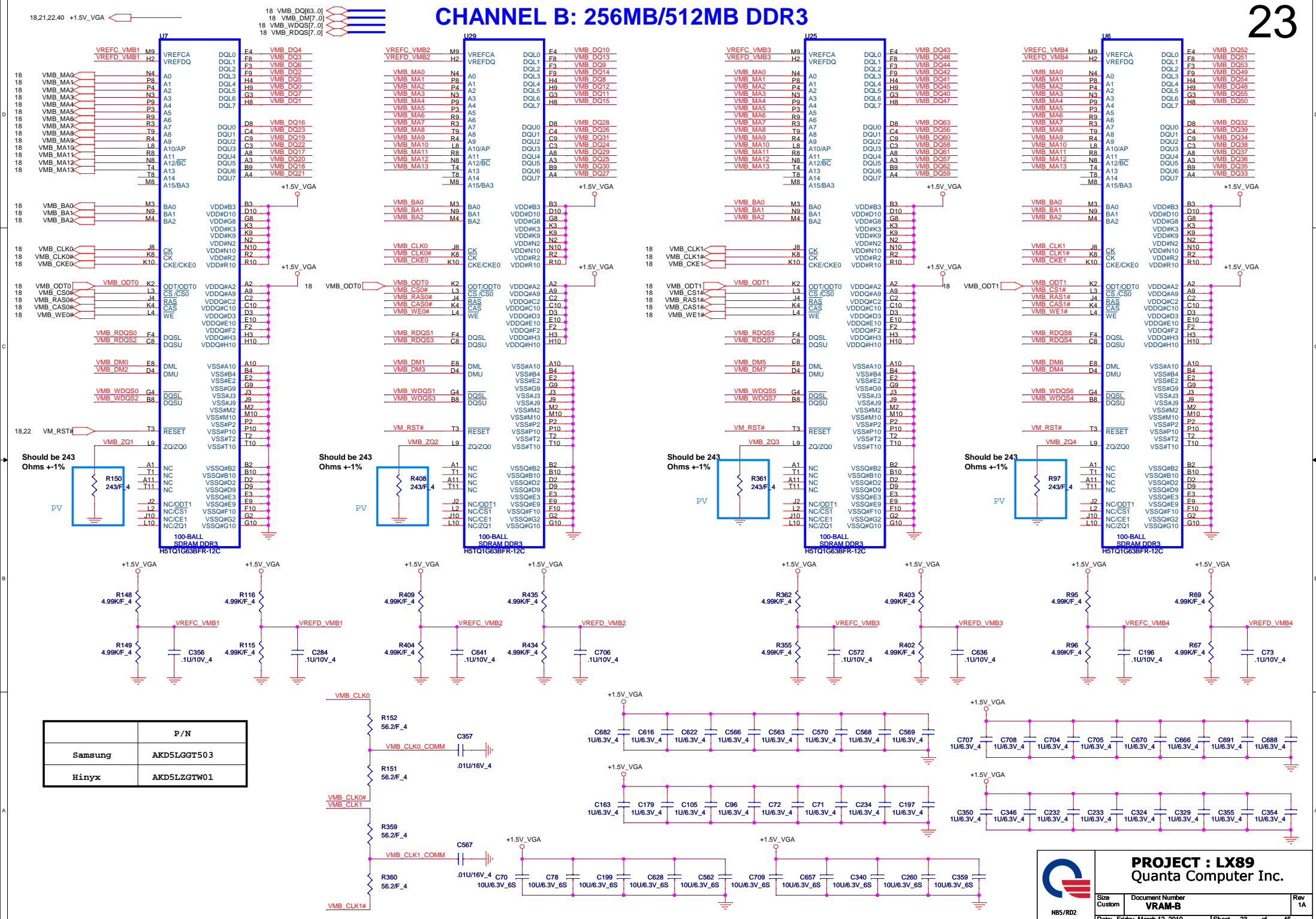


Size Custom	Document Number ATI Park/Madison(GND&Str&Ther)4/5	Rev 1A
Date: Friday, March 12, 2010		Sheet 20 of 45

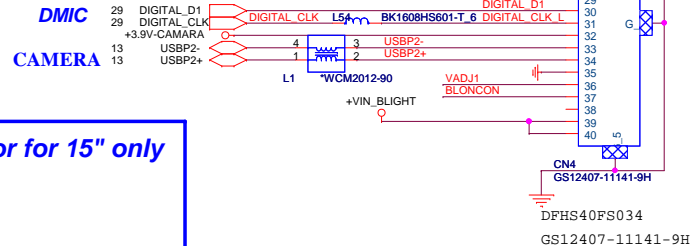
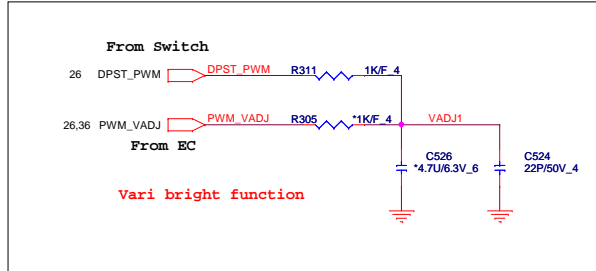
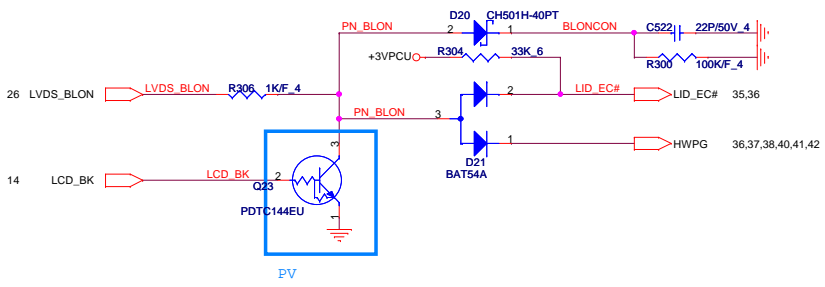
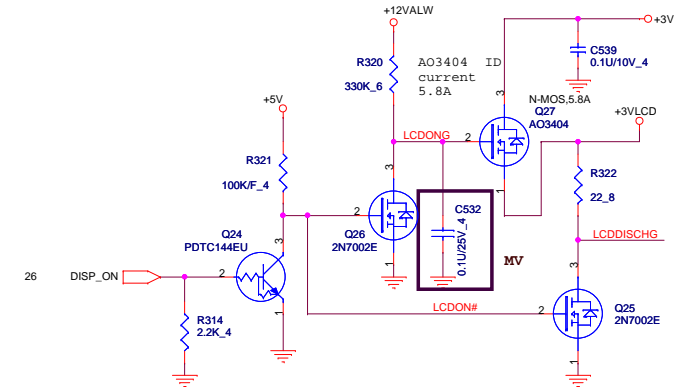
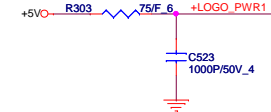
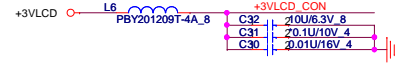
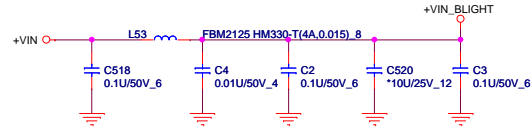




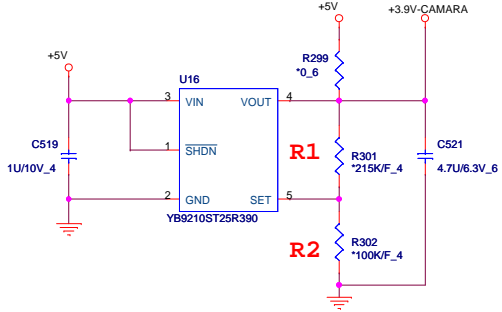
CHANNEL B: 256MB/512MB DDR3



+VIN	28,31,37,38,39,40,41,42,43
+12VALW	33,35,40,41,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,41,42
+3V_DELAY	12,18,19,20,21,26,27
+5V	25,26,27,28,29,33,34,35,42

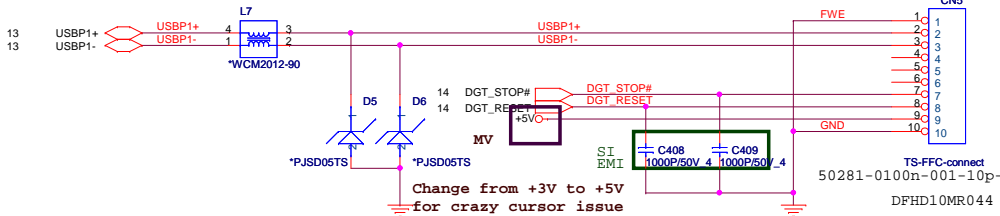


CAMERA POWER



$$V_{out} = 1.25(1 + R1/R2)$$

Digitizer Connector for 15" only

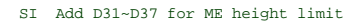


$$V_{out} = 1.25(1 + R1/R2)$$

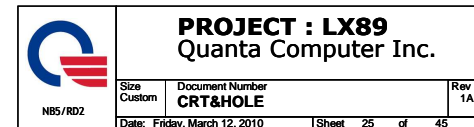
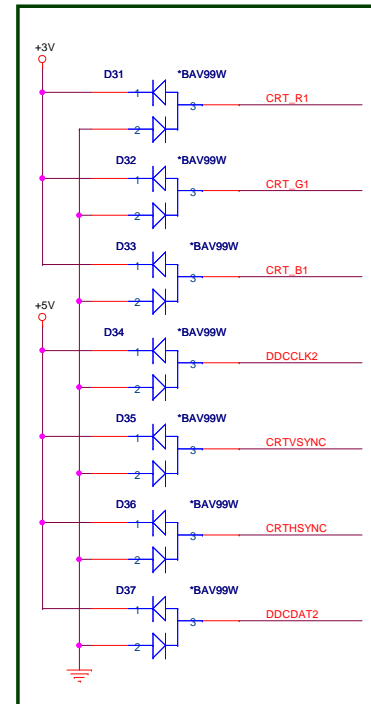
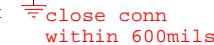
	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number LCD CONN Date: Friday, March 12, 2010	Rev 1A Sheet 24 of 45

+3V	2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,41,42
+5V	24,26,27,28,29,33,34,35,42
+3V_DELAY	12,18,19,20,21,26,27

PV Change footprint for ME concern ^{+5VCRT}

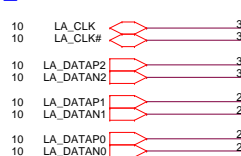


25

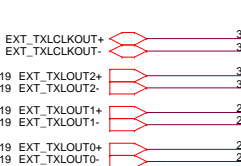
26 VSYNC_COM ☐

For Single-link panel

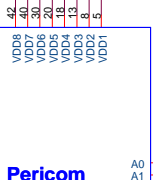
IGPU_Channel-A



DGPU_Channel-A



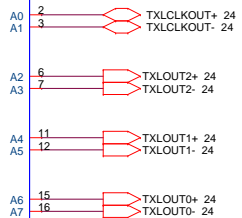
LVDS Channel Switch



SELx	Ay
HIGH	B2
LOW	B1

Pericom

PI2PCIE412-DZHE



SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

LVDS Channel Switch



Pericom

PI2PCIE412-DZHE



SELx	Ay
HIGH	B2
LOW	B1

Pericom

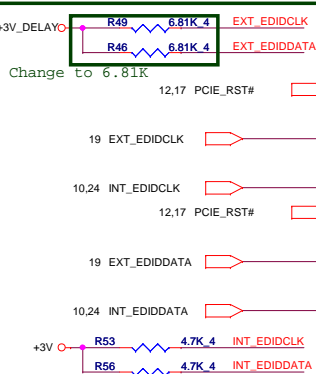
PI2PCIE412-DZHE



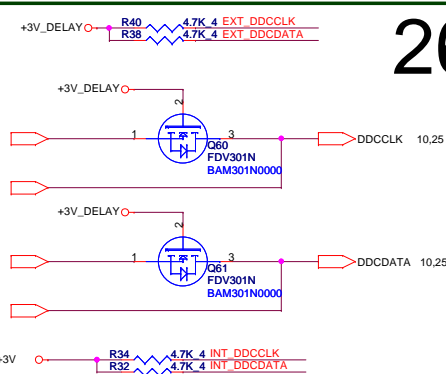
SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

OPTION SIGNAL FROM NB to LVDS for UMA			
LA_CLK	1	2	TXCLKOUT+
LA_CLK#	3	4	TXCLKOUT-
LA_DATA0	RP10	2	*0_4P2R_4 TXLOUT0+
LA_DATA0#	RP13	4	*0_4P2R_4 TXLOUT0-
LA_DATA1	RP11	2	*0_4P2R_4 TXLOUT1+
LA_DATA1#	RP12	4	*0_4P2R_4 TXLOUT1-
LA_DATA2	RP11	2	*0_4P2R_4 TXLOUT2+
LA_DATA2#	RP7	4	*0_4P2R_4 TXLOUT2-
LB_CLK	1	2	TXCLKOUT+
LB_CLK#	3	4	TXCLKOUT-
LB_DATA0	RP6	2	*0_4P2R_4 TXUOUT0+
LB_DATA0#	RP9	4	*0_4P2R_4 TXUOUT0-
LB_DATA1	RP3	2	*0_4P2R_4 TXUOUT1+
LB_DATA1#	RP8	4	*0_4P2R_4 TXUOUT1-
LB_DATA2	RP3	2	*0_4P2R_4 TXUOUT2+
LB_DATA2#	RP7	4	*0_4P2R_4 TXUOUT2-

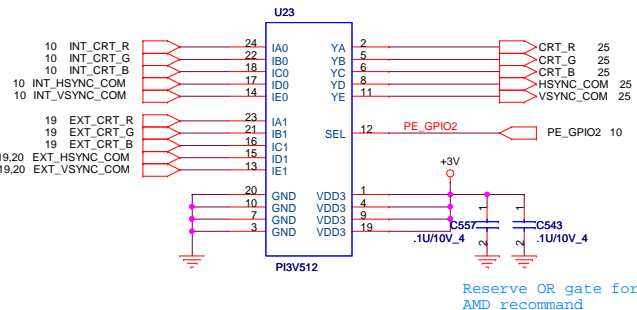
LVDS/CRT DDC Switch



Change to 6.81K

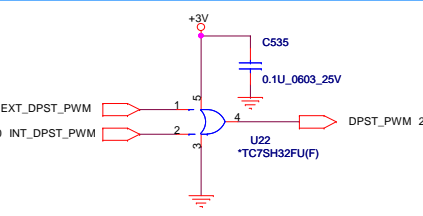


VGA Switch



OPTION SIGNAL FROM NB to CRT for UMA

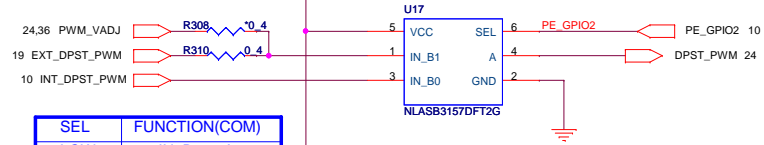
INT_CRT_R	R342	*0_4	CRT_R
INT_CRT_G	R341	*0_4	CRT_G
INT_CRT_B	R340	*0_4	CRT_B
INT_HSVMCOM	3	4	HSVMCOM
INT_VSYNC_COM	1	2	VSYNC_COM



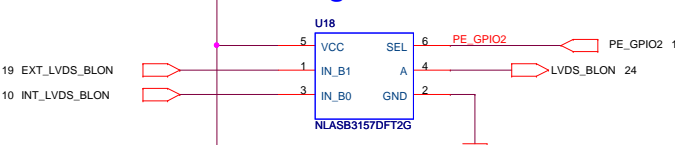
OPTION DPST SIGNAL FROM NB to LVDS for UMA

INT_DPST_PWM	R312	*0_4	DPST_PWM
--------------	------	------	----------

DPST Control



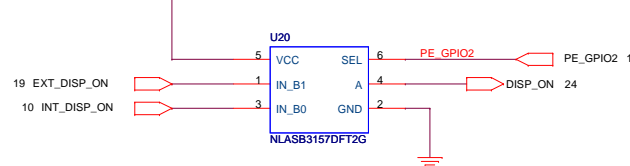
Back Light On control



OPTION Back Light SIGNAL FROM NB to LVDS for UMA

INT_LVDS_BLOn	R313	*0_4	LVDS_BLOn
---------------	------	------	-----------

LCDVcc control



OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

INT_DISP_ON	R318	*0_4	DISP_ON
-------------	------	------	---------

PROJECT : LX89
Quanta Computer Inc.

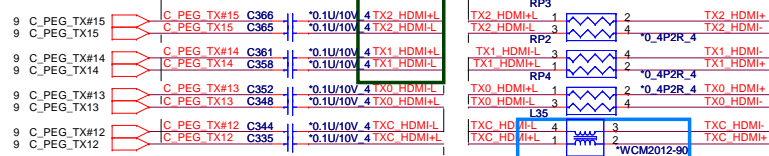
Size	Document Number	Rev
Custom	LVDS/CRT Hyper_switch	1A
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UMA/DISCRETE select for HDMI

From RS880M

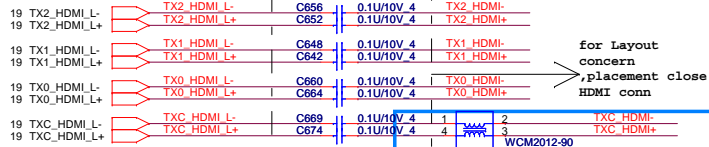
for Layout
concern
,placement close
north bridge

SI



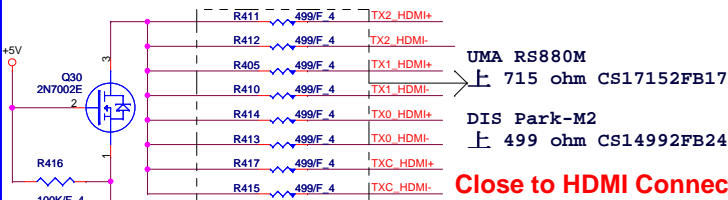
PV for EMI

From Park-M2



WCM2012-90

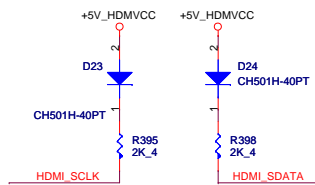
PV for EMI



UMA RS880M
└ 715 ohm CS17152FB17

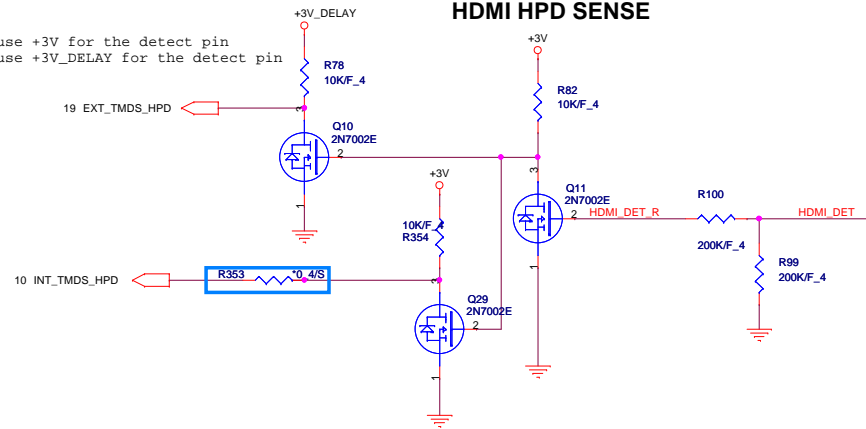
DIS Park-M2
└ 499 ohm CS14992FB24

Close to HDMI Connector



+5V 24,25,26,28,29,33,34,35,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,28,29,30,31,32,33,34,35,36,41,42
+3V_DELAY 12,18,19,20,21,26

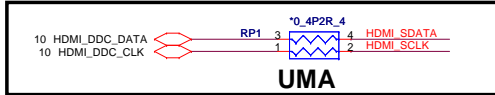
UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



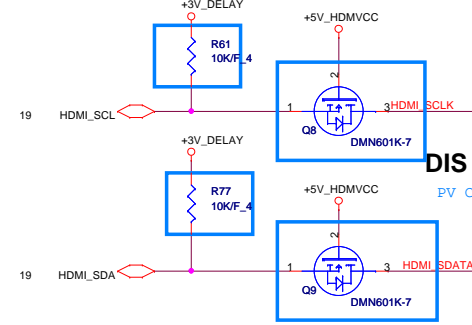
HDMI HPD SENSE

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector



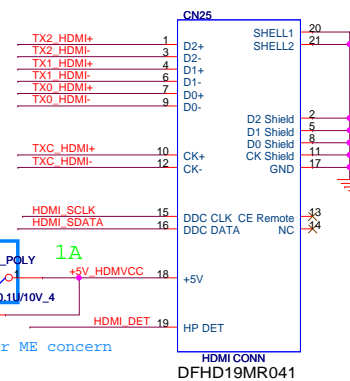
UMA



DIS

PV Change to 10K and MOS for HDMI issue

HDMI PORT



PV Change footprint for ME concern

CN25

SHELL1

SHELL2

D2+

D2-

D1+

D1-

D0+

D0-

CK+

CK-

DDC CLK

CE Remote

DDC DATA

HP DET

HDMI CONN

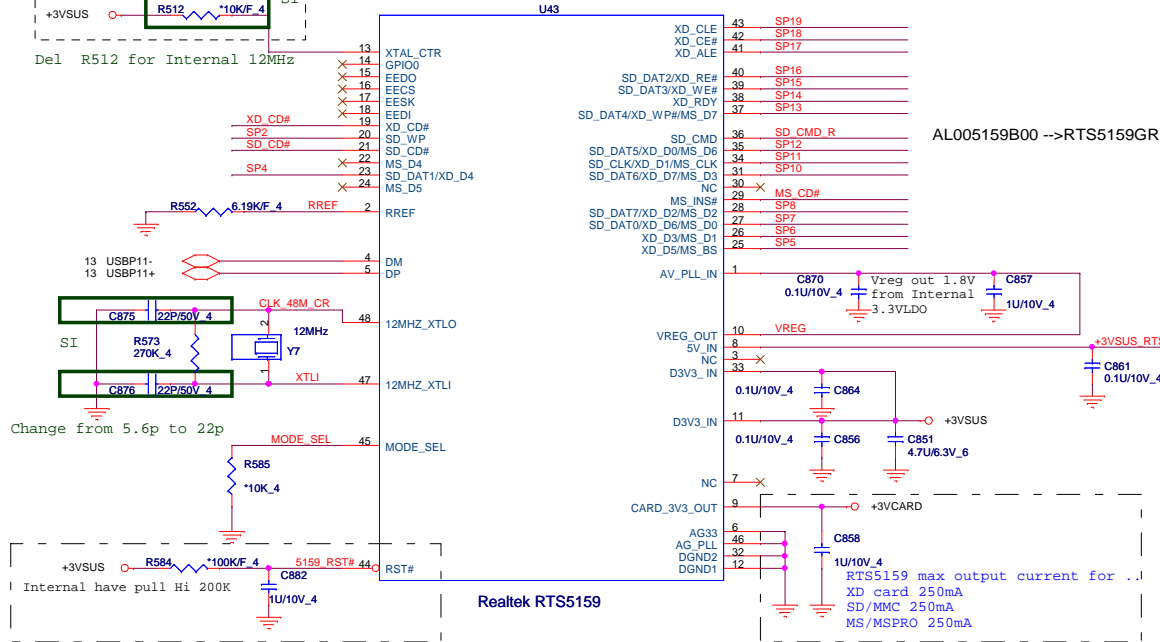
DFHD19MR041

hdmi-100042gr019s168-19p-1dv-v

XTAL control pin for
12Mhz crystal or 48Mhz
clk in

+3VSUS \rightarrow R512 \rightarrow 10K/F_4 SI

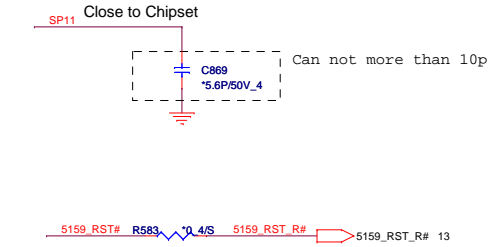
Del R512 for Internal 12MHz



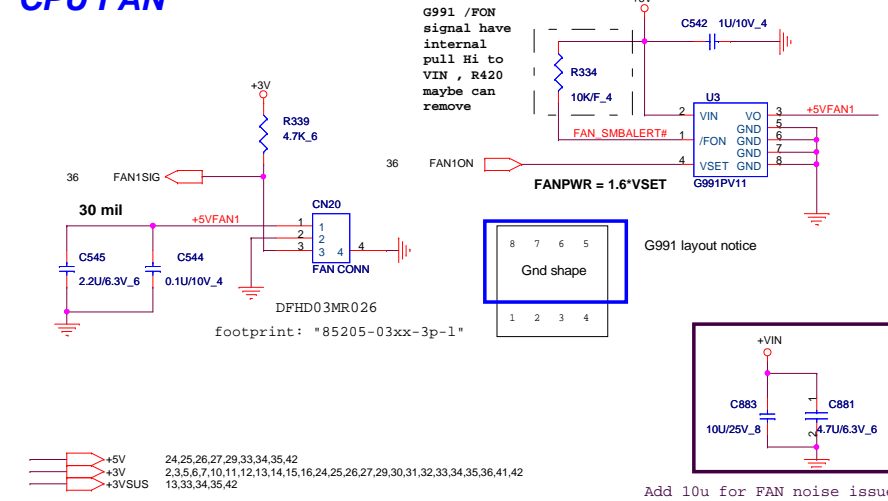
Note:

SD/MMC	MS	XD
SP1	SD_WP	XD_CD#
SP2	SD_CD#	
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5	MS_BS	XD D5
SP6	MS_D1	XD D3
SP7	SD_DAT0	MS D0
SP8	SD_DAT7	MS D2
SP9	MS_INS#	XD D7
SP10	SD_DAT6	MS D3
SP11	SD_CLK	MS SCLK
SP12	SD_DAT5	XD D0
SP13	SD_DAT4	XD WP#
SP14		XD R/B#
SP15	SD_DAT3	XD WE#
SP16	SD_DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

PV	DEL	OR
SP7		MS-D0 SD-D0 XD-D6
SP6		MS-D1 XD-D3 SD-D1
SP8		MS-D2 XD-D2
SP16		XD-RE# SD-D2
SP5		MS-BS XD-D5
SP15		SD-D3 XD-WE
SP11		SD_CLK MS_CLK
SP2		SD_WP
SP13		XD-WP#
SP19		XD-CLE
SP4		XD-D4
SP10		MS-D3 XD-D7
SP14		XD-RB#
SP12		XD-D0
SP17		XD-ALE
SP18		XD-CE#
SD_CMD_R		SD-CMD



CPU FAN



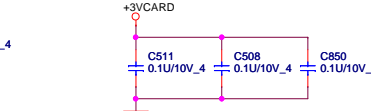
SI Modify CN15 footprint for SMT issue

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

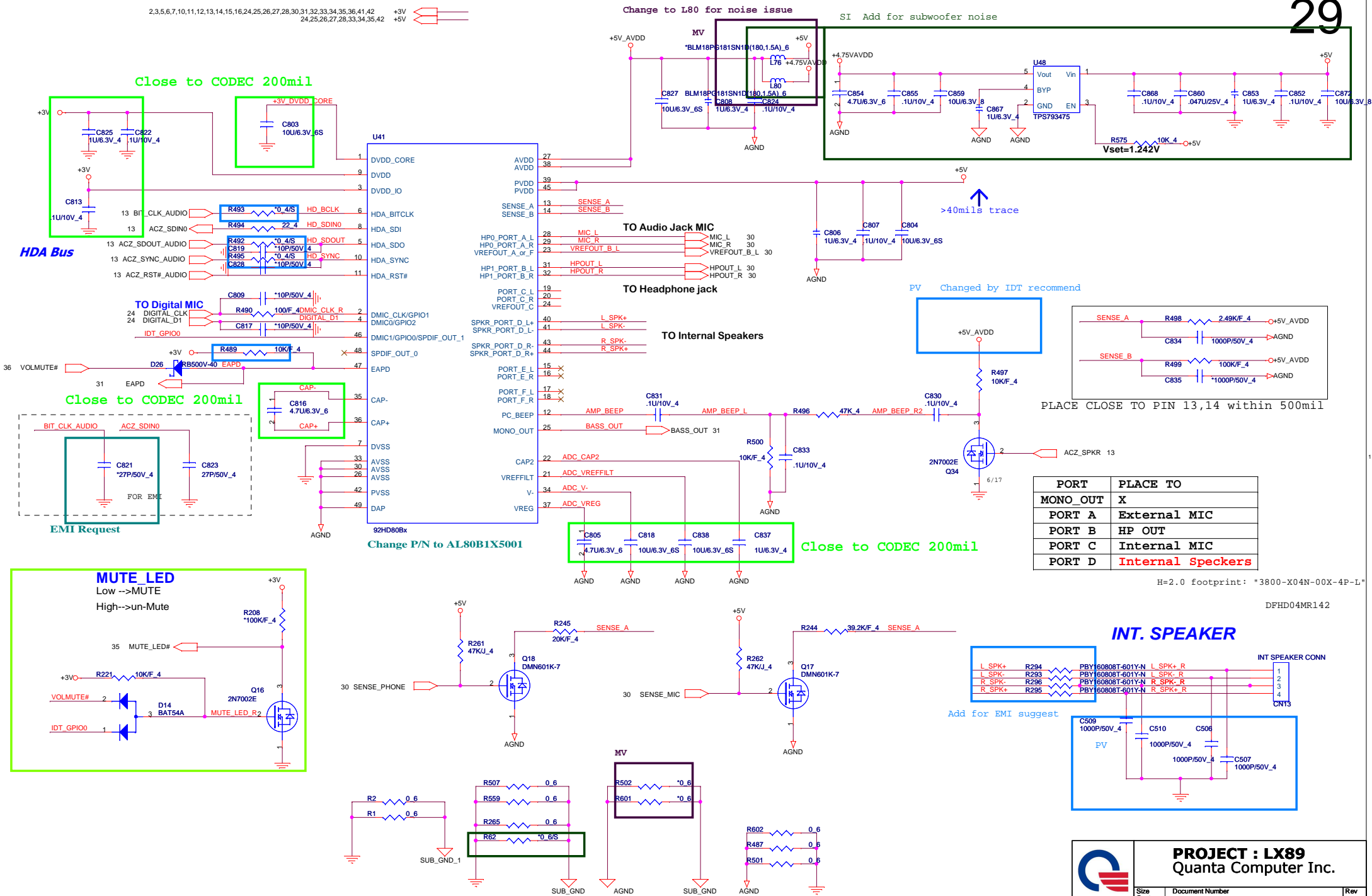
DFHD36MR005

4in1-cm4s-205-36p-r-v

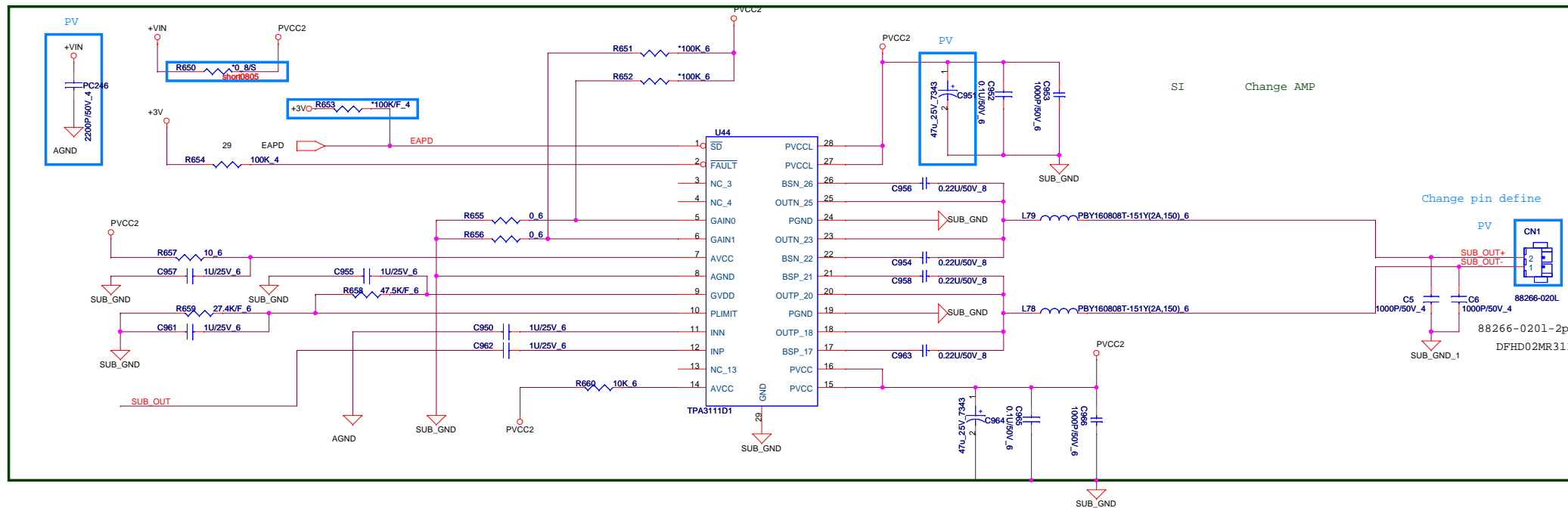
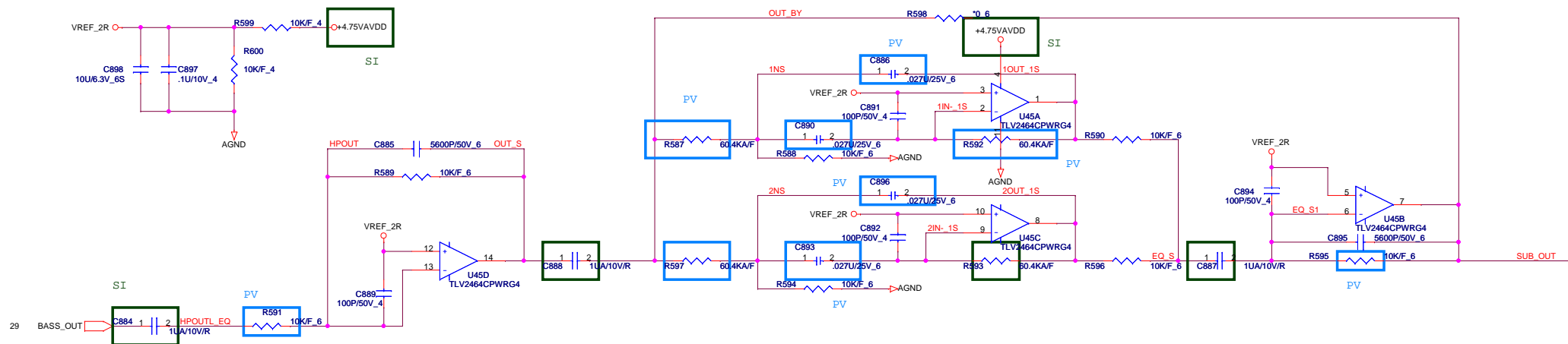


PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159&CPU FAN	1A
Date: Friday, March 12, 2010	Sheet 28	of 45



EQ FOR SUBWOOFER



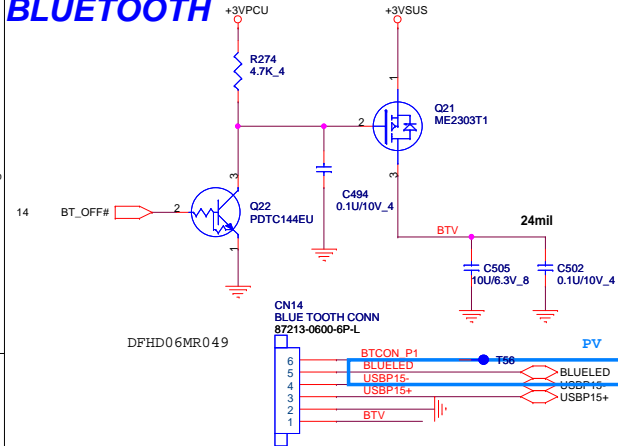
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,41,42
 +4.75VAVDD 29
 +VIN 24,28,37,38,39,40,41,42,43



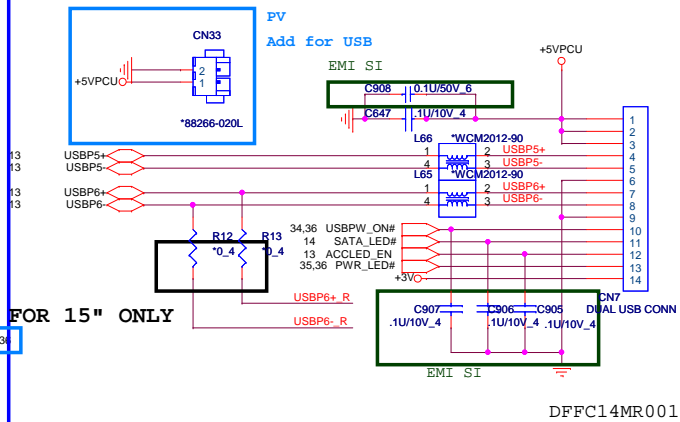
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	1A
Date: Friday, March 12, 2010		Sheet 31 of 45

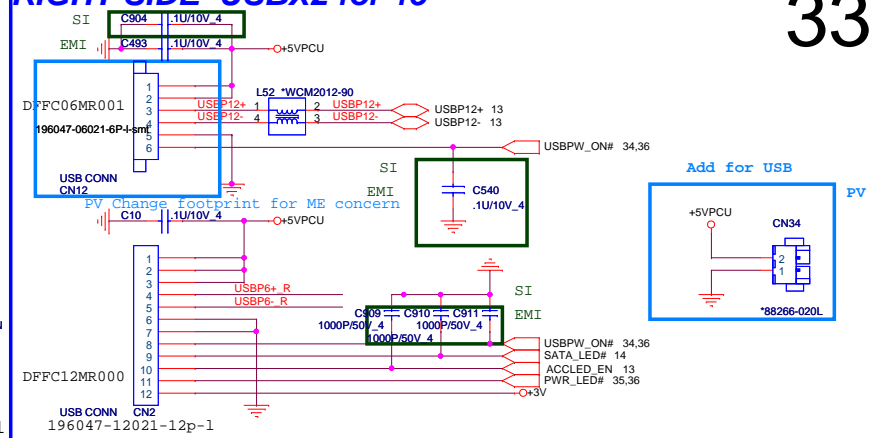
BLUETOOTH



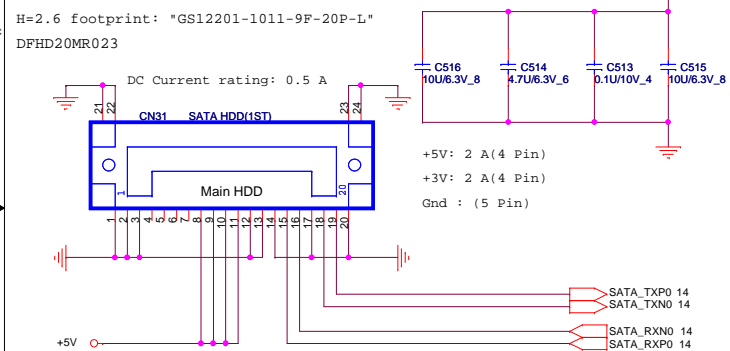
RIGHT SIDE USBX2 for 17"



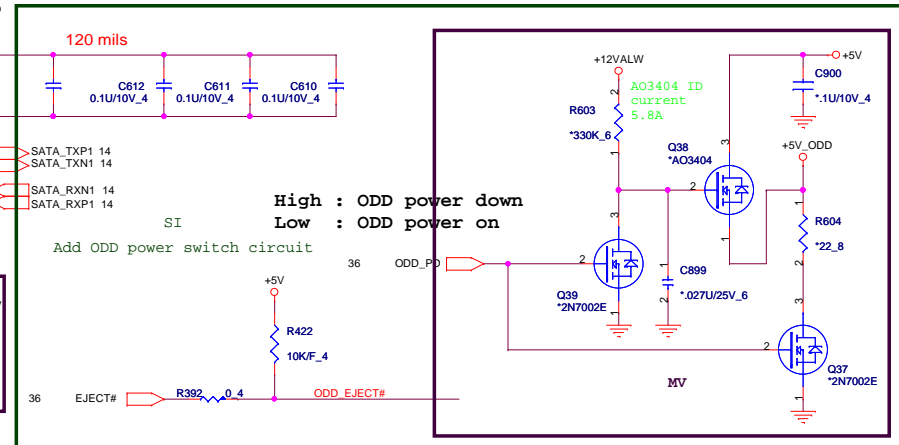
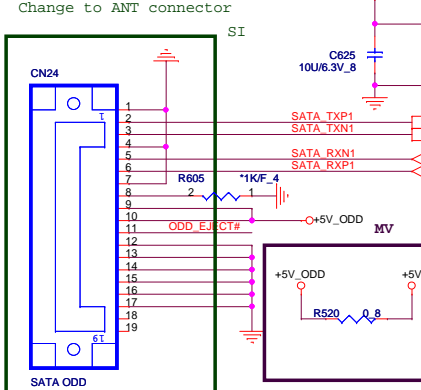
RIGHT SIDE USBX2 for 15"



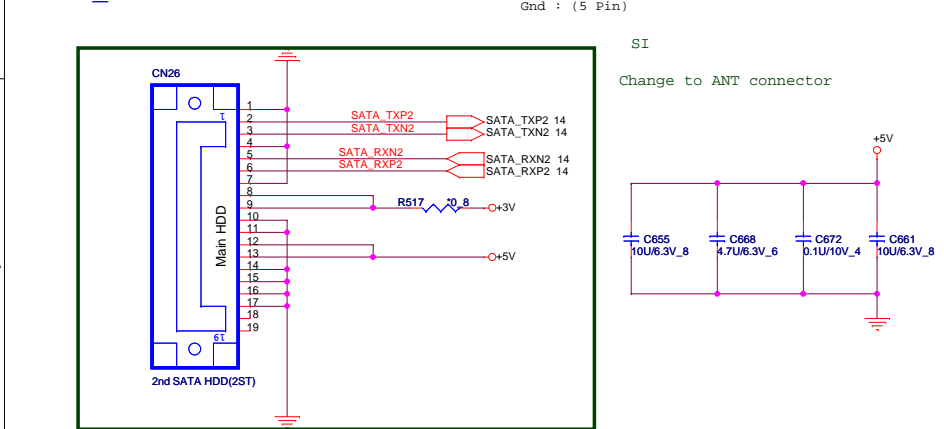
SATA HDD CONNECTOR



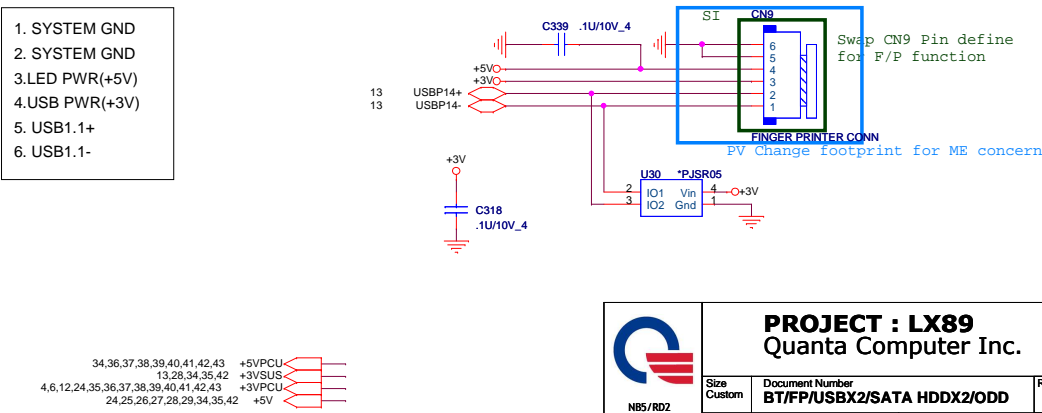
SATA CD-ROM



SATA_2 HDD CONNECTOR FOR 17.3"

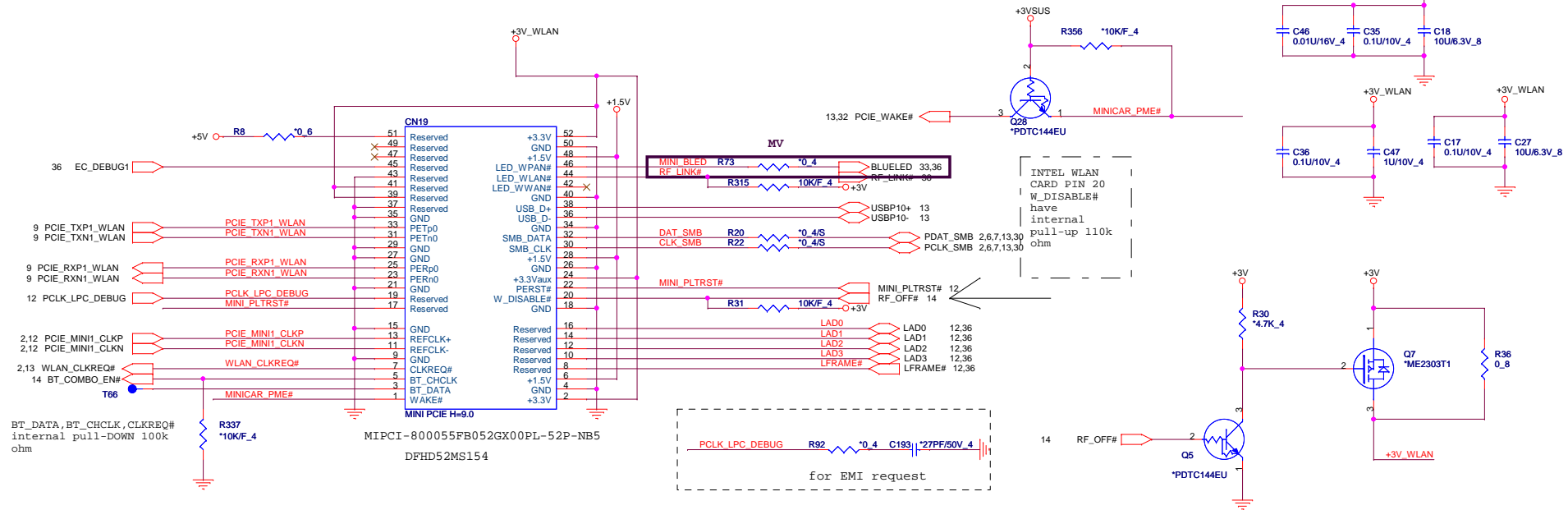


USB Fingerprint CON

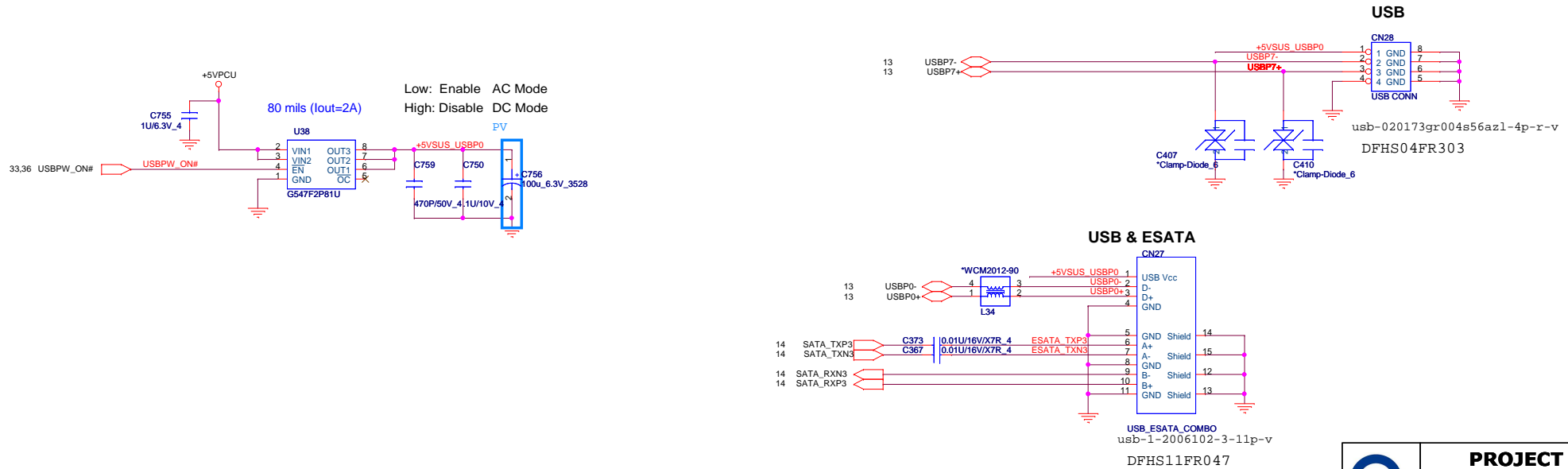


Mini PCI-E Card WLAN

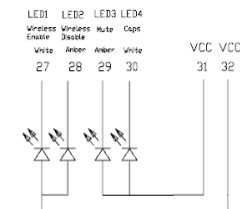
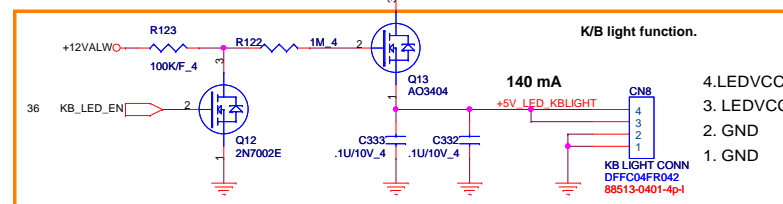
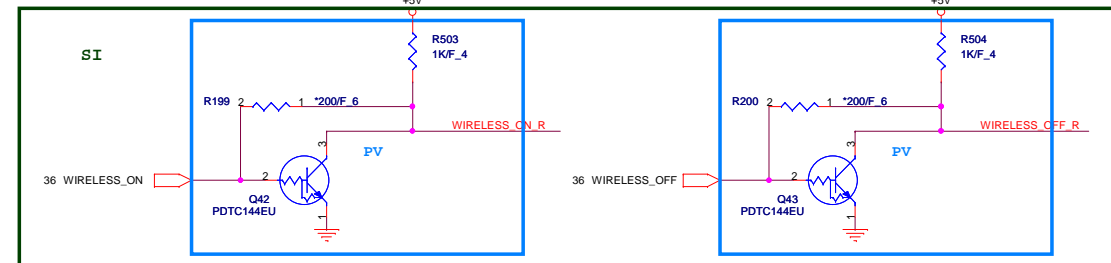
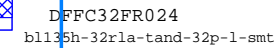
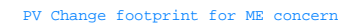
34



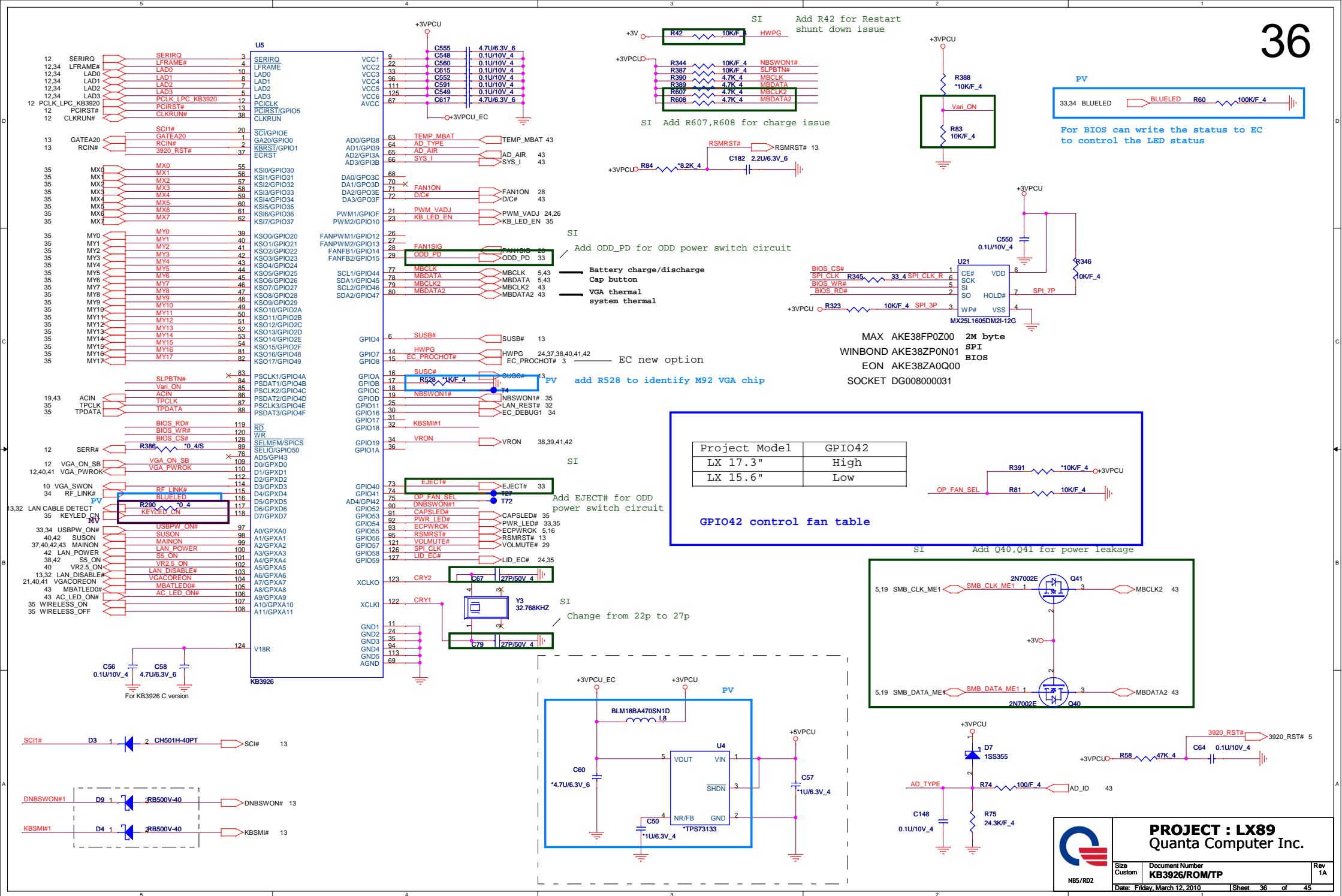
USB2.0 X 1 and E-SATA/USB2.0 COMBO



TOUCH PAD CONN

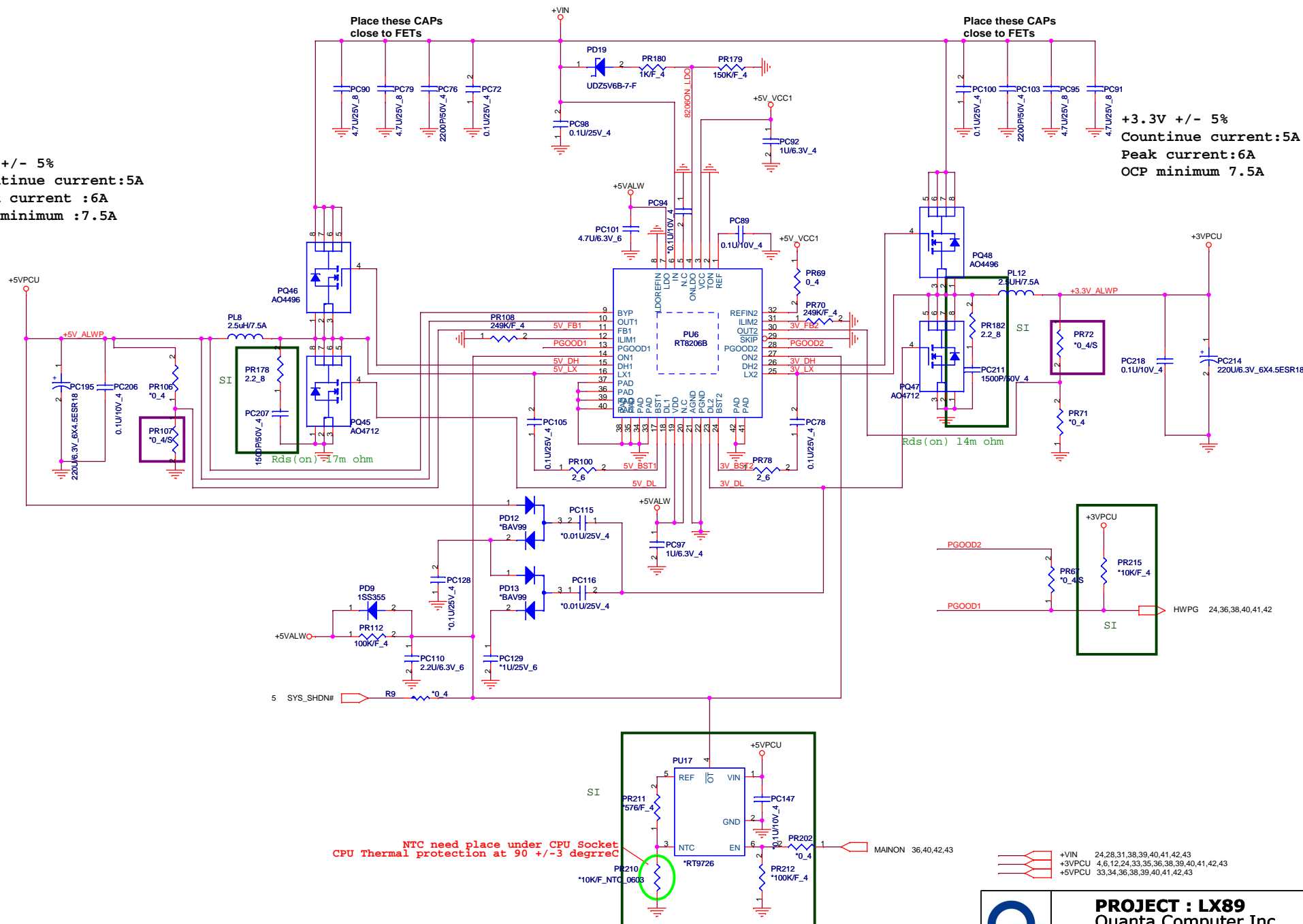


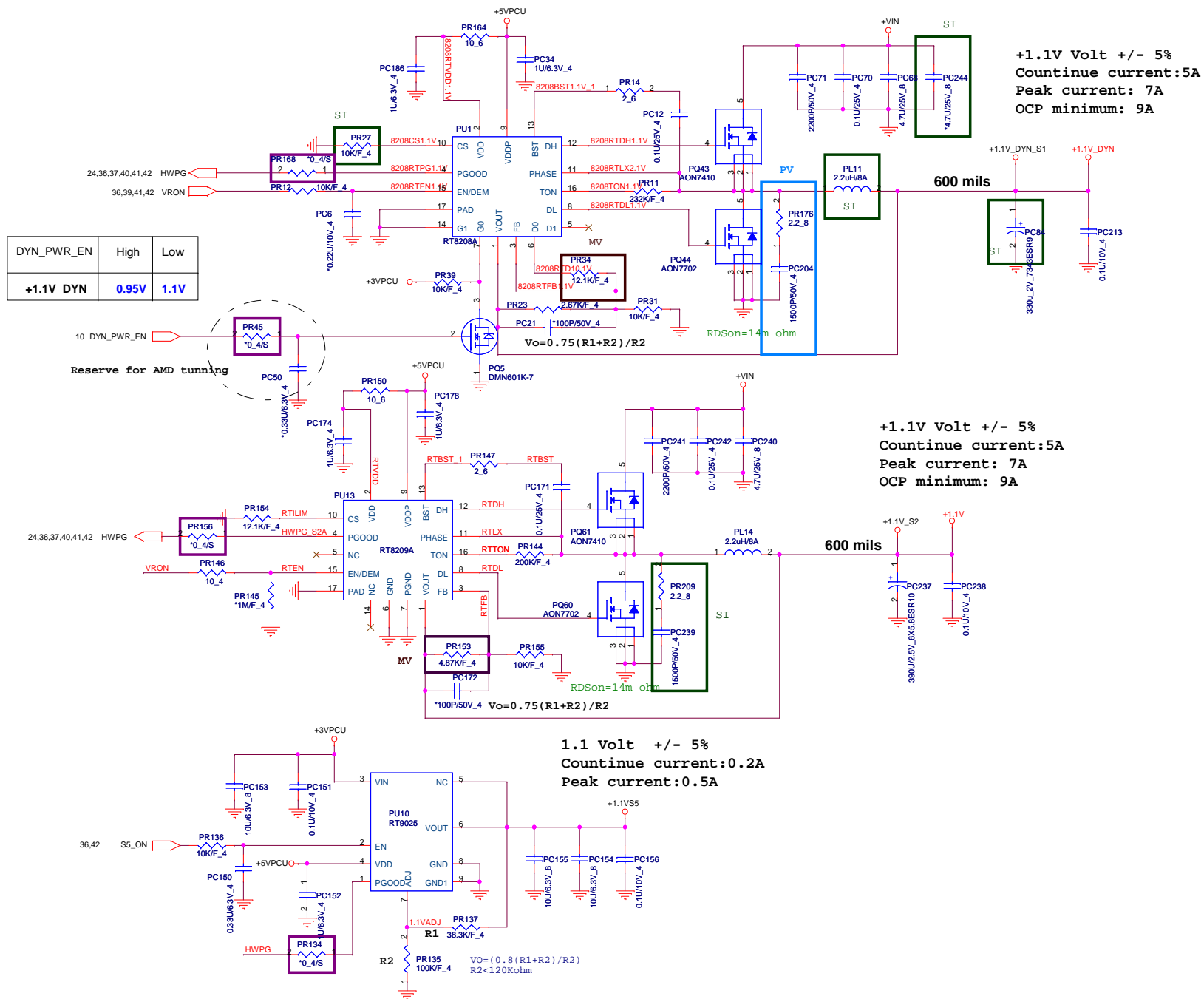
12		30	112		58	119	56		51		13	123		62	126	76	91	94	
1		110	115	127	35	118	125		36		41	122	107		15	75	92	95	
8	58	16	114		21	117	28		22		27	121			90	80	93	96	
9		1	113	70	6	116	45	59	7		12	120	129	$\frac{29}{46}$	85	101	97		
5	64	31	33	71	34	32	38		37		40	39			43	86	106	104	
6		46	48	72	49	47	53		52	44	55	54			61	81	100	103	
3		2	4	73	5	3	9		8		11	10			60	84	89	99	102
2		17	19	74	20	18	24		23	57	26	25			83	79	105	108	
7	11	13	18	14	10	17	15		16	4	23	22	19	20	21	24	25	26	



+5V +/- 5%
 Countinue current:5A
 Peak current :6A
 OCP minimum :7.5A

+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A

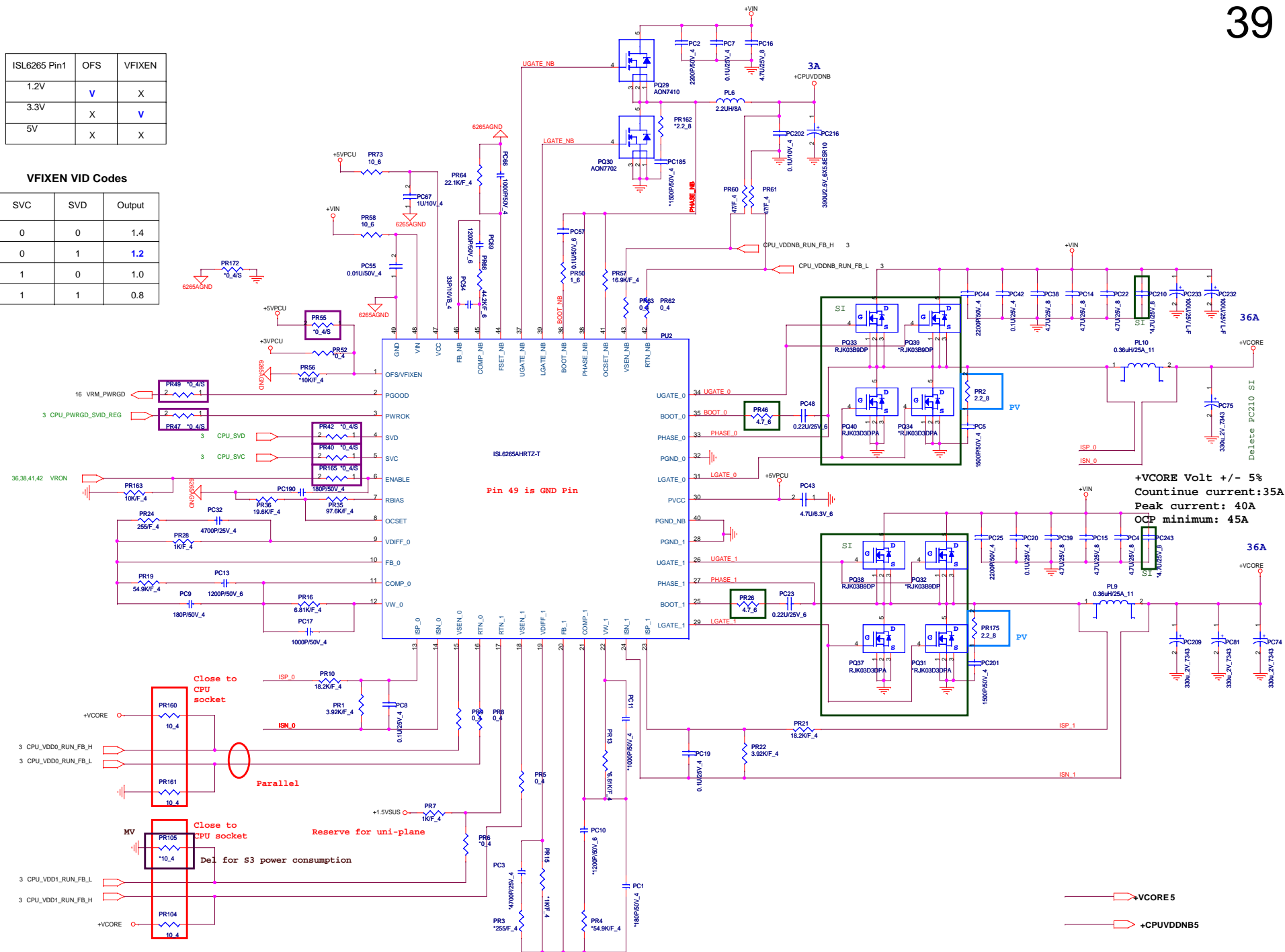




ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



47

VGA Core

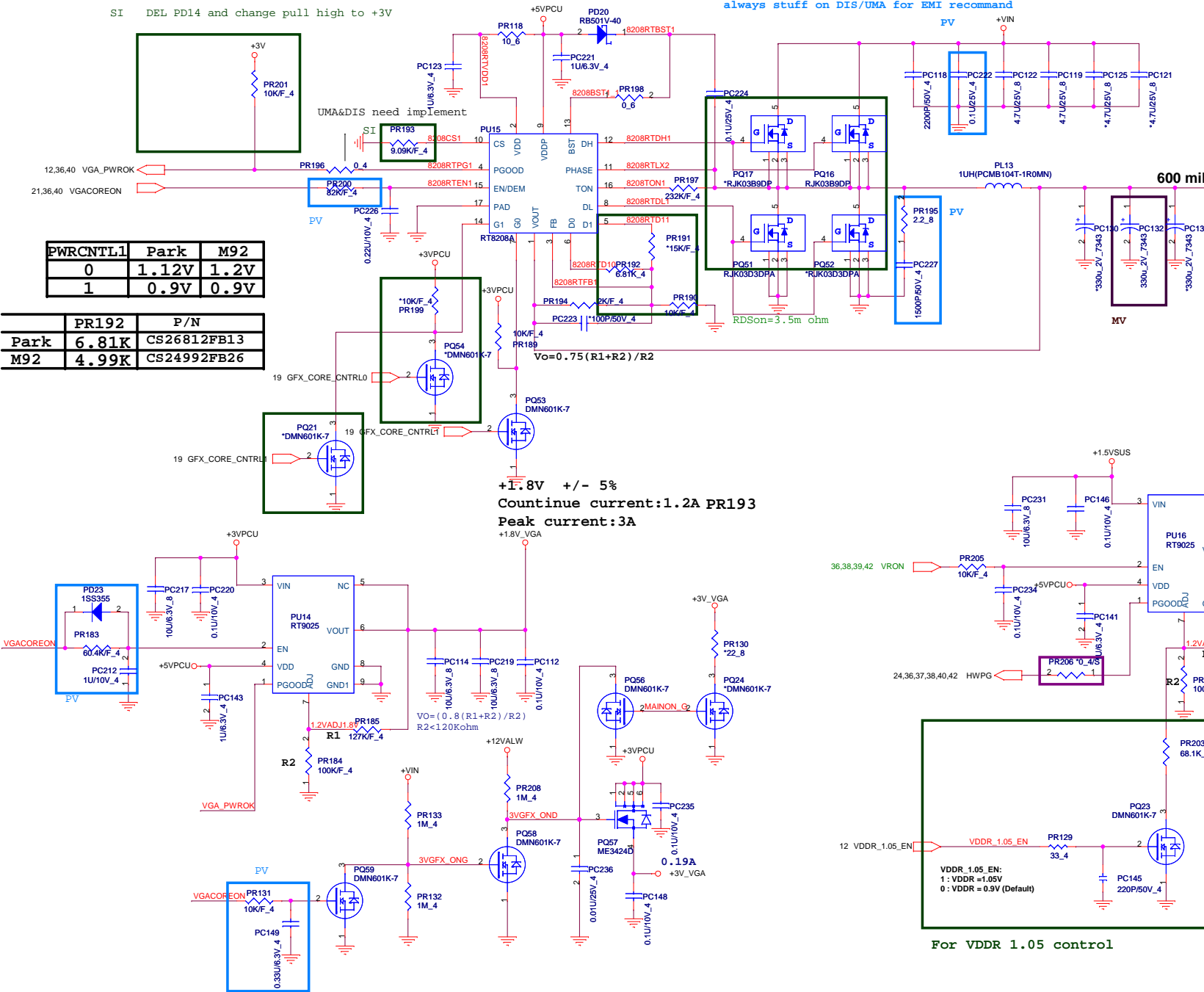
SI DEL PD14 and change pull high to +3V

always stuff on DIS/UMA for EMI recommend

+VGACORE +/- 5%
 Countinue current:11A
 Peak current:16A
 PARK OCP minimum:17A

PWRCNTL1	Park	M92
0	1.12V	1.2V
1	0.9V	0.9V

	PR192	P/N
Park	6.81K	CS26812FB13
M92	4.99K	CS24992FB26



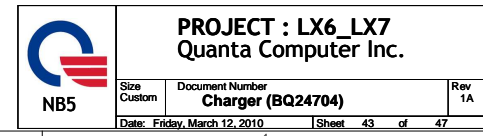
600 mils

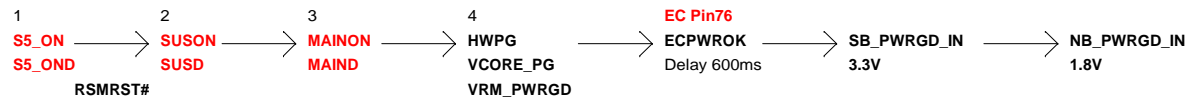
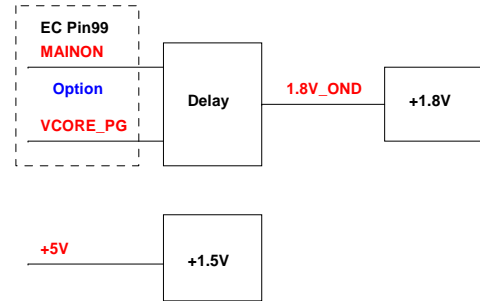
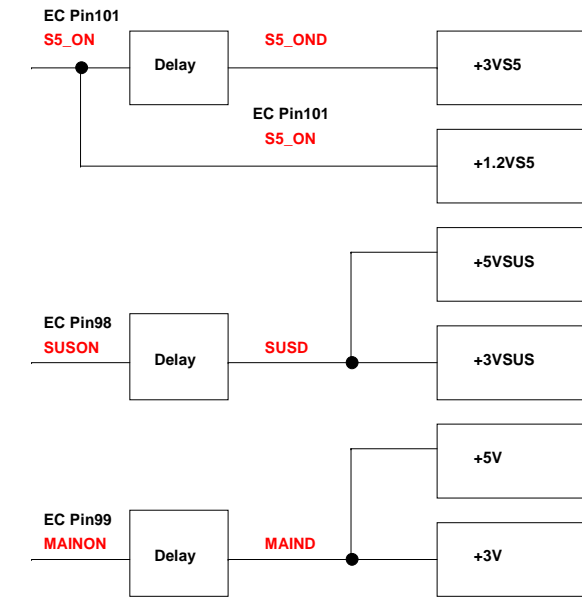
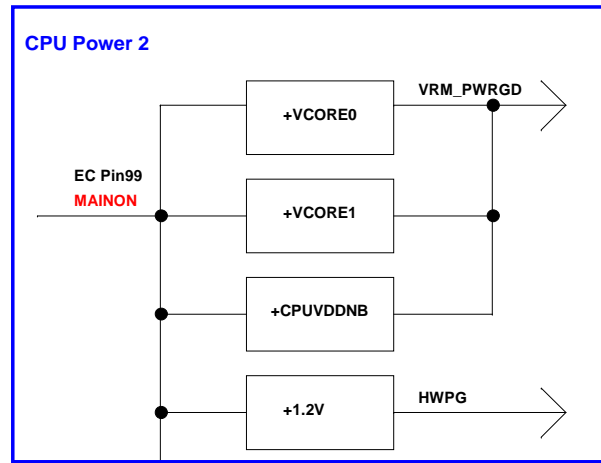
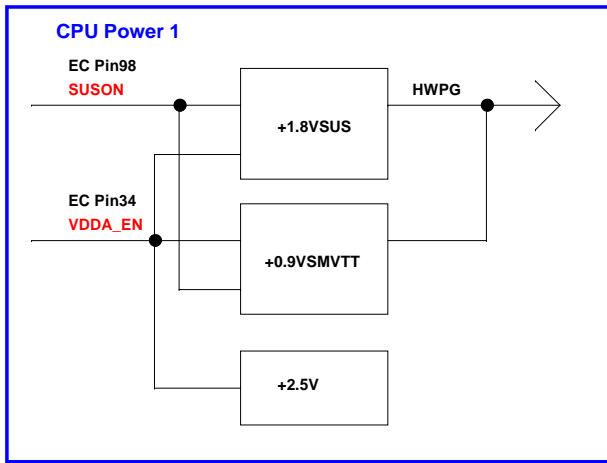
+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

SI
 Del U33,PC147,PR202 for No support
 MEM_1.5V function

For VDDR 1.05 control

20346-100n-1-10p-ldv





Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT