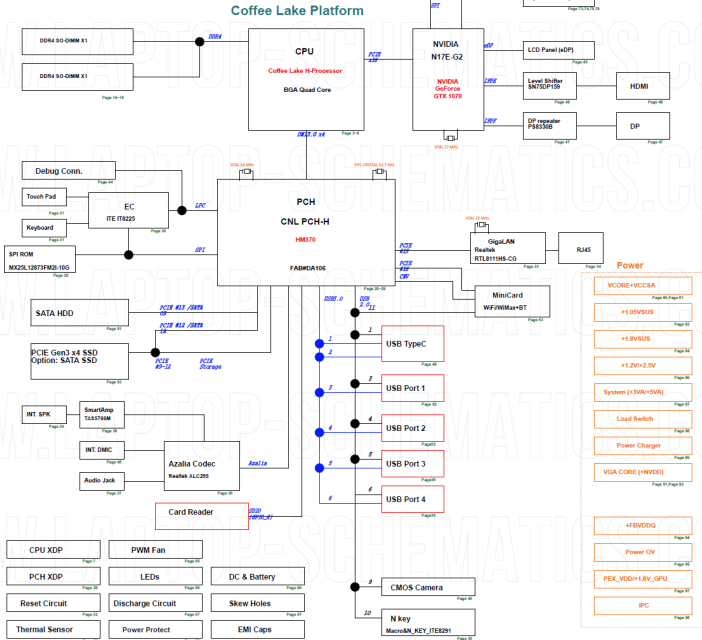


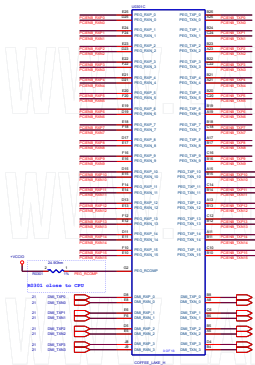
HM170-SR2C4 6代
HM270-SR30W 7代
SR40B 8代

GL703GS Block Diagram



01. Block Diagram
02. System Setting
03. CPU_FMS/FMS/adP/DSI
04. CPU_DIMM
05. CPU_GND
06. CPU_CPG/RSVD
07. CPU_XDP
08. CPU_PWR
09. CPU_FMR
10. CPU_POWER_CAP
11. DIMM_DDR4 SO-DIMM A1
12. DIMM_DDR4 SO-DIMM B1
13. DIMM_CA/DQ Voltage
14. VCH_HDA_SMD_SYS_PWR_VTAC
15. PCH_PCIE SATA, USB2, MISC
16. PCH_CLK_LPC_USB3
17. PCH-CPT(4) adP_PCI_DP
18. PCH-CPT(5) LPC_SPI_SMBIOS
19. PCH_GSTIO
20. PCH_POWER_GND
21. PCH_POWER_GND
22. PCH-INT_HDM_OTG
23. PCH_XDP
24. PCH_ITB225
25. PCH_HS & TP
26. RST_Reset Circuit
27. LAN RTL8111HS-G
28. LAN_R454 Conn.
29. MacroN_KEY_I7ER291
30. AUDIO_ALC3234-CG/VB2
31. AUDIO_ALC3234-CG/VB2 Jack
32. Aud_HP Jack, MIC
33. Aud_Woofar
34. MiniCard_SSD
35. CB_CONN
36. DSR02_LIC
37. CPT_40P
38. Display Port Conn.
39. HDAE
40. Type C Port
41. FAN_Thermal Sensor & Fan
42. XDP_HDD & HDD_CONN
43. USB_Charger
44. NGFF_Type_WLAN/ST
45. LED_Indicator
46. USB_Charge
47. Power_Protect
48. DC & BAT_IM
49. I/O board_PUNC key
50. OTG_BMT
51. GPU_PCIE I/F
52. GPU_POWER
53. GPU_POWER_HOPPER
54. VRAM-CHANNEL A
55. VRAM-CHANNEL B
56. VRAM-CHANNEL C
57. VRAM-CHANNEL D
58. VRAM_CAP
59. GPU_CLOCK/STAMP/GPIO
60. GPU_INT_HDM/HDMI
61. PW_CPGCORE
62. PW_VCCPGCORE
63. PW_+1.0VDS
64. PW_+1.8VDS
65. PW_+1.2V/VTT/+2.5V
66. PW_+3.3VDS
67. PW_LOAD_SWITCH
68. PW_CHARGER
69. PW_PROTECTION
70. PW_+MVDDQ (1)
71. PW_+MVDDQ (2)
72. PW_+MVDDQ
73. PW_+PBVDDQ
74. PW_+1.2VDS_FAN
75. PW_LPC
76. PW_FLOW_CHART
77. Power On Timing-AC mode
78. Power On Timing-DC mode
79. Power On Timing-GPU
80. Clock Distribution Diagram
81. SMBIOS Block Diagram
82. Power Distribution Diagram

PCIEG



Notes to CPU-4 Bus P.155 (000-570000)

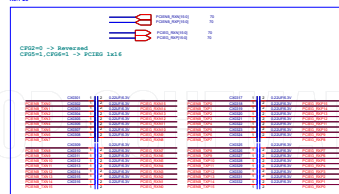
Table 2-13. PCI Express® Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals		Lanes															
	W10	W11	W12	CFG [0]	CFG [1]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1x8	x16	N/A	N/A	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Reversed																					
2x8	x8	x8	N/A	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Reversed																					
1x8+2x4	x8	x4	x4	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Reversed																					

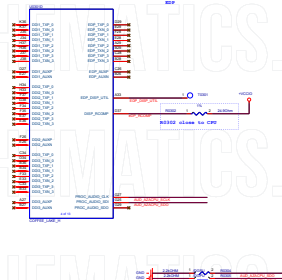
Notes:

- For CFG bus details, refer to Section 6.4.
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.
- For example:
 - A. When using 1x8 + 2x4, the 8 lane device should use lanes 0-7.
 - B. When using 2x4 + 1x2, the 4 lane device should use lanes 0-3, and other 2 lanes device should use lanes 8-9.
 - C. When using 1x4 + 1x2 + 1x2, 4 lane device should use lanes 0-3, two lane device should use lanes 8-9, one lane device should use lane 12.
- For reversal lanes, for example:
 - When using 1x8, the 8 lane device should use lanes 8-15, so lane 15 will be connected to lane 0 of the Device.
- For Base Platform use 1x8+2x4 Bifurcation.

RS-1-05



Display



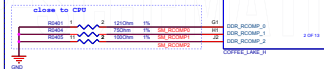
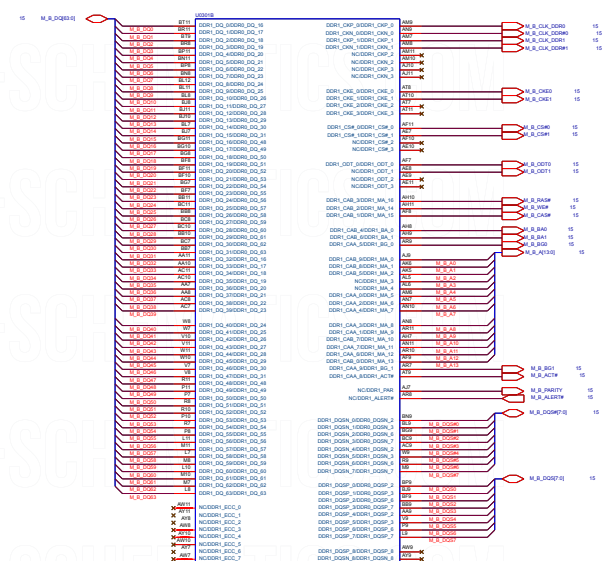
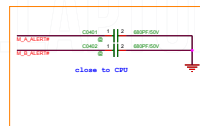
Refer to CPU-4 Pin P.143 (000-571340)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA, SDI[1:0], DISPA, SDI0 interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ). PROC_AUDIO_SDO can be left unconnected.

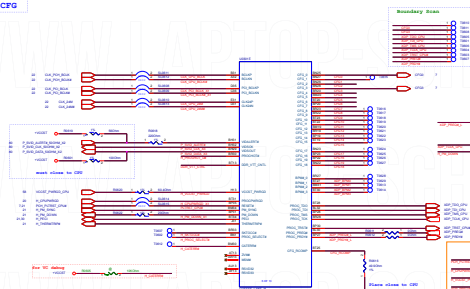
Memory Channel B



Rev	
-----	--

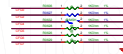


CFG



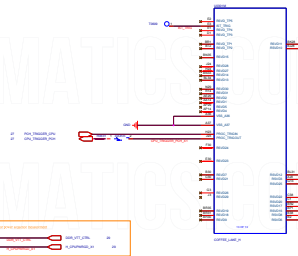
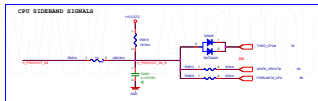
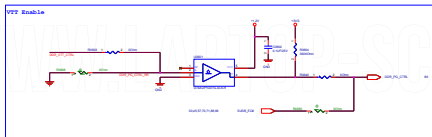
CFG Straps

Main Board



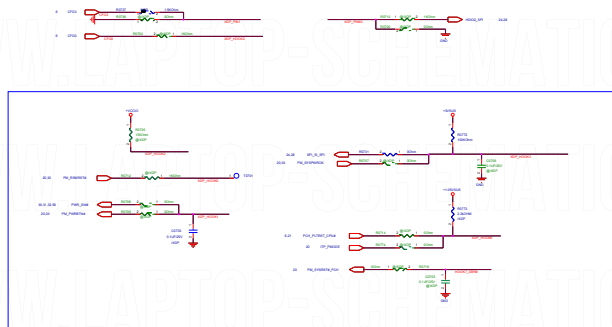
CFG Straps for Processor
CFG0: Boot/Reset/Exception after PCI/PLX SCLX USB as assertion 1. CPU/PLX SCLX USB as assertion 2. Boot/Reset/Exception after PCI/PLX SCLX USB as assertion
CFG1: Reserved Configuration Lanes Reserved Configuration Lanes
CFG2: PCI Express® Mode with Lane Numbering Reserved 1. Reserved Configuration Lanes 2. Lane Numbering Reserved
CFG3: Reserved Configuration Lanes Reserved Configuration Lanes
CFG4: Reserved Configuration Lanes Reserved Configuration Lanes
CFG5: Reserved Configuration Lanes Reserved Configuration Lanes
CFG6: Reserved Configuration Lanes Reserved Configuration Lanes
CFG7: Reserved Configuration Lanes Reserved Configuration Lanes
CFG8: Reserved Configuration Lanes Reserved Configuration Lanes
CFG9: Reserved Configuration Lanes Reserved Configuration Lanes
CFG10: Reserved Configuration Lanes Reserved Configuration Lanes
CFG11: Reserved Configuration Lanes Reserved Configuration Lanes
CFG12: Reserved Configuration Lanes Reserved Configuration Lanes
CFG13: Reserved Configuration Lanes Reserved Configuration Lanes
CFG14: Reserved Configuration Lanes Reserved Configuration Lanes
CFG15: Reserved Configuration Lanes Reserved Configuration Lanes
CFG16: Reserved Configuration Lanes Reserved Configuration Lanes
CFG17: Reserved Configuration Lanes Reserved Configuration Lanes
CFG18: Reserved Configuration Lanes Reserved Configuration Lanes
CFG19: Reserved Configuration Lanes Reserved Configuration Lanes
CFG20: Reserved Configuration Lanes Reserved Configuration Lanes
CFG21: Reserved Configuration Lanes Reserved Configuration Lanes
CFG22: Reserved Configuration Lanes Reserved Configuration Lanes
CFG23: Reserved Configuration Lanes Reserved Configuration Lanes
CFG24: Reserved Configuration Lanes Reserved Configuration Lanes
CFG25: Reserved Configuration Lanes Reserved Configuration Lanes
CFG26: Reserved Configuration Lanes Reserved Configuration Lanes
CFG27: Reserved Configuration Lanes Reserved Configuration Lanes
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CFG30: Reserved Configuration Lanes Reserved Configuration Lanes
CFG31: Reserved Configuration Lanes Reserved Configuration Lanes
CFG32: Reserved Configuration Lanes Reserved Configuration Lanes
CFG33: Reserved Configuration Lanes Reserved Configuration Lanes
CFG34: Reserved Configuration Lanes Reserved Configuration Lanes
CFG35: Reserved Configuration Lanes Reserved Configuration Lanes
CFG36: Reserved Configuration Lanes Reserved Configuration Lanes
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CFG38: Reserved Configuration Lanes Reserved Configuration Lanes
CFG39: Reserved Configuration Lanes Reserved Configuration Lanes
CFG40: Reserved Configuration Lanes Reserved Configuration Lanes
CFG41: Reserved Configuration Lanes Reserved Configuration Lanes
CFG42: Reserved Configuration Lanes Reserved Configuration Lanes
CFG43: Reserved Configuration Lanes Reserved Configuration Lanes
CFG44: Reserved Configuration Lanes Reserved Configuration Lanes
CFG45: Reserved Configuration Lanes Reserved Configuration Lanes
CFG46: Reserved Configuration Lanes Reserved Configuration Lanes
CFG47: Reserved Configuration Lanes Reserved Configuration Lanes
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CFG50: Reserved Configuration Lanes Reserved Configuration Lanes
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CFG57: Reserved Configuration Lanes Reserved Configuration Lanes
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CFG60: Reserved Configuration Lanes Reserved Configuration Lanes
CFG61: Reserved Configuration Lanes Reserved Configuration Lanes
CFG62: Reserved Configuration Lanes Reserved Configuration Lanes
CFG63: Reserved Configuration Lanes Reserved Configuration Lanes
CFG64: Reserved Configuration Lanes Reserved Configuration Lanes
CFG65: Reserved Configuration Lanes Reserved Configuration Lanes
CFG66: Reserved Configuration Lanes Reserved Configuration Lanes
CFG67: Reserved Configuration Lanes Reserved Configuration Lanes
CFG68: Reserved Configuration Lanes Reserved Configuration Lanes
CFG69: Reserved Configuration Lanes Reserved Configuration Lanes
CFG70: Reserved Configuration Lanes Reserved Configuration Lanes
CFG71: Reserved Configuration Lanes Reserved Configuration Lanes
CFG72: Reserved Configuration Lanes Reserved Configuration Lanes
CFG73: Reserved Configuration Lanes Reserved Configuration Lanes
CFG74: Reserved Configuration Lanes Reserved Configuration Lanes
CFG75: Reserved Configuration Lanes Reserved Configuration Lanes
CFG76: Reserved Configuration Lanes Reserved Configuration Lanes
CFG77: Reserved Configuration Lanes Reserved Configuration Lanes
CFG78: Reserved Configuration Lanes Reserved Configuration Lanes
CFG79: Reserved Configuration Lanes Reserved Configuration Lanes
CFG80: Reserved Configuration Lanes Reserved Configuration Lanes
CFG81: Reserved Configuration Lanes Reserved Configuration Lanes
CFG82: Reserved Configuration Lanes Reserved Configuration Lanes
CFG83: Reserved Configuration Lanes Reserved Configuration Lanes
CFG84: Reserved Configuration Lanes Reserved Configuration Lanes
CFG85: Reserved Configuration Lanes Reserved Configuration Lanes
CFG86: Reserved Configuration Lanes Reserved Configuration Lanes
CFG87: Reserved Configuration Lanes Reserved Configuration Lanes
CFG88: Reserved Configuration Lanes Reserved Configuration Lanes
CFG89: Reserved Configuration Lanes Reserved Configuration Lanes
CFG90: Reserved Configuration Lanes Reserved Configuration Lanes
CFG91: Reserved Configuration Lanes Reserved Configuration Lanes
CFG92: Reserved Configuration Lanes Reserved Configuration Lanes
CFG93: Reserved Configuration Lanes Reserved Configuration Lanes
CFG94: Reserved Configuration Lanes Reserved Configuration Lanes
CFG95: Reserved Configuration Lanes Reserved Configuration Lanes
CFG96: Reserved Configuration Lanes Reserved Configuration Lanes
CFG97: Reserved Configuration Lanes Reserved Configuration Lanes
CFG98: Reserved Configuration Lanes Reserved Configuration Lanes
CFG99: Reserved Configuration Lanes Reserved Configuration Lanes
CFG100: Reserved Configuration Lanes Reserved Configuration Lanes

DDR_VTT_CTRL
System Memory Power Mode Control:
Enables the platform memory VTT regulator in C8 and deeper and S1.

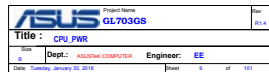


ASUS	Model: G6700GS	Rev: 1.0
Part:	CPU G6700GS	
Rev:	1.0	
Eng:	ASUS	Eng: 68

Main Board



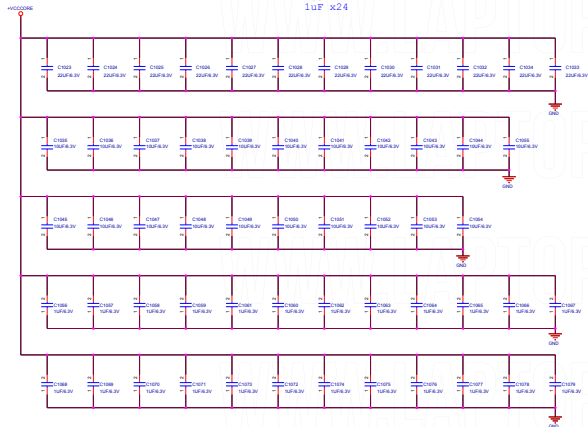




Main Board

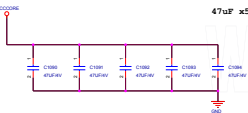
+VCCCORE DECAPS Place Back Side (TOP)

22uF x12
10uF x21
1uF x24

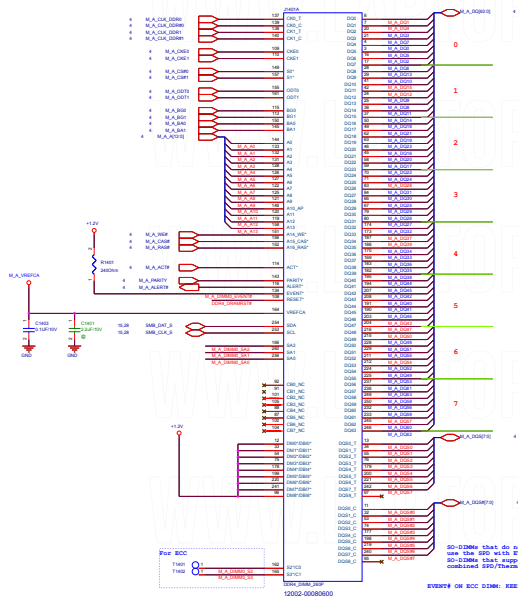


+VCCCORE cap near CPU

47uF x5

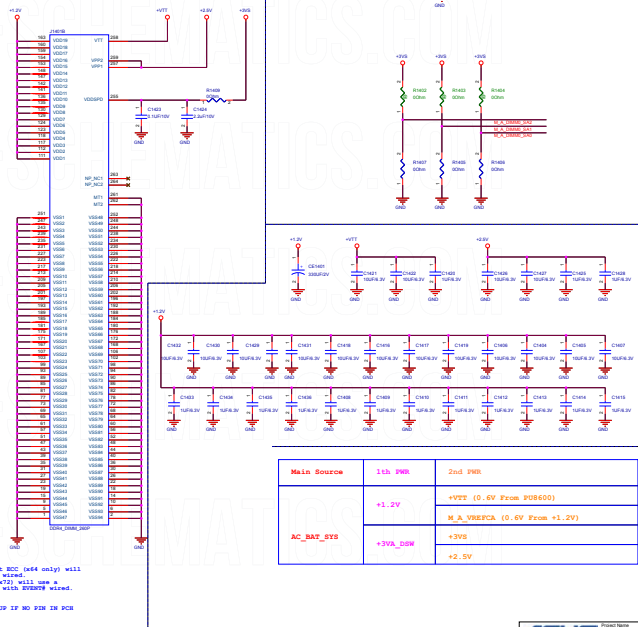


12002-00080600
DDR4 DIMM 260P 4H REV



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with WUEN# wired.

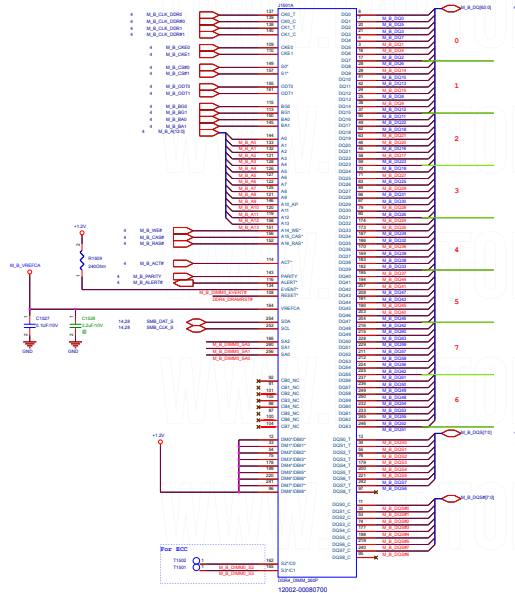
EVENT# ON ECC DIMM: KEEP A POLL UP IF NO PIN IN PCU



Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From P0B600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

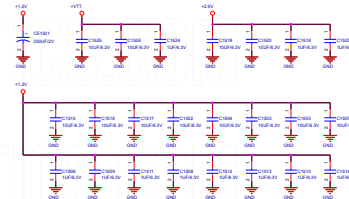
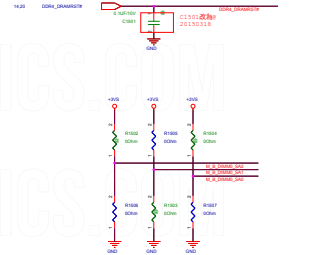
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00080700
DDR4 DIMM 260P 4H STD



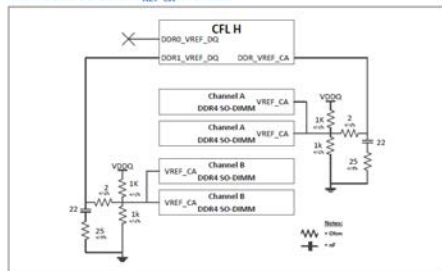
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combi SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN SCH

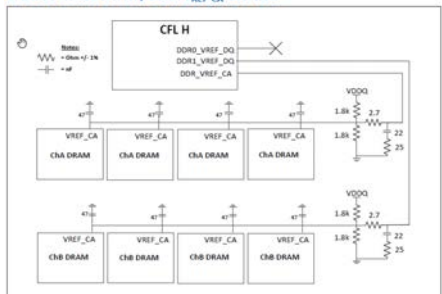


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PWS600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

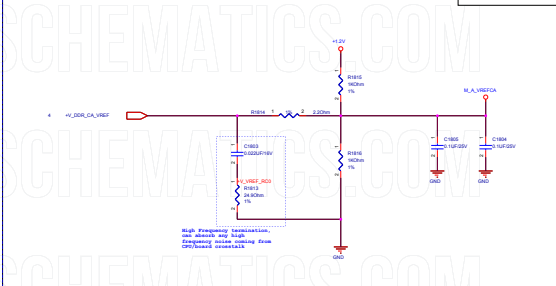
CFL'H DDR4 SO-DIMM V_{REF-CA} Overview



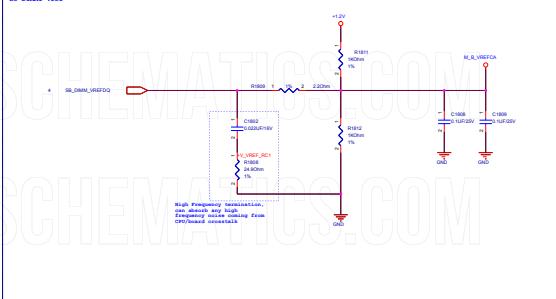
CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



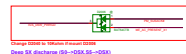
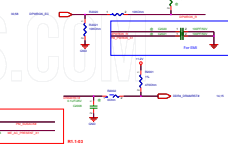
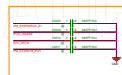
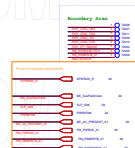
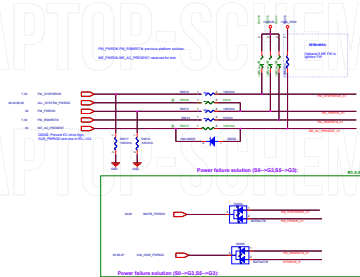
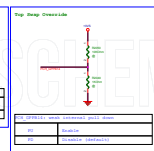
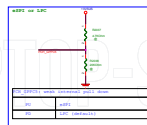
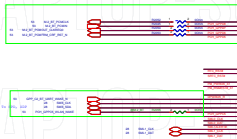
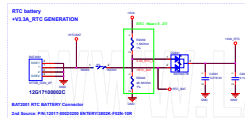
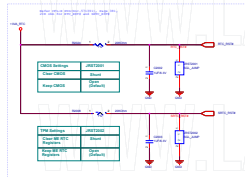
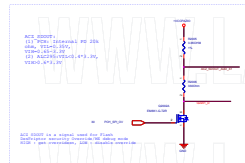
SO-D1280 Vref

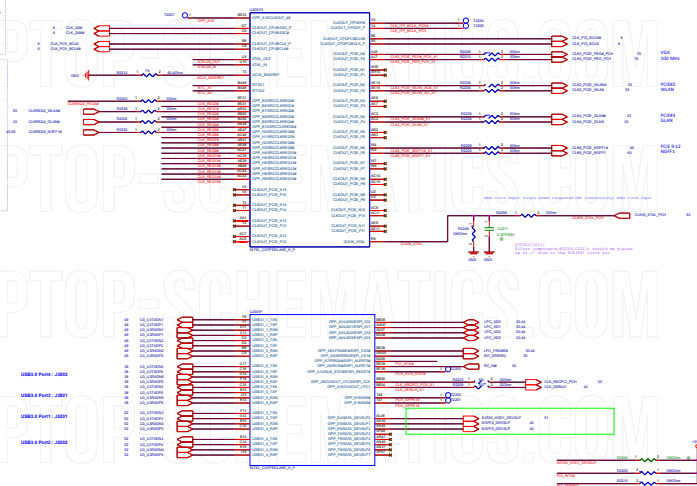
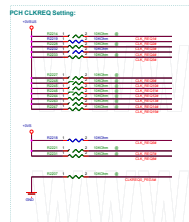
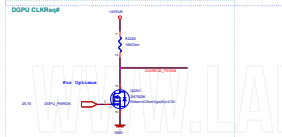
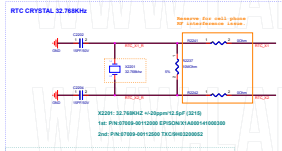
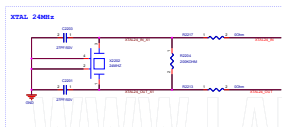


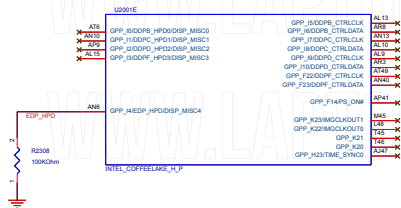
SO-D1281 Vref



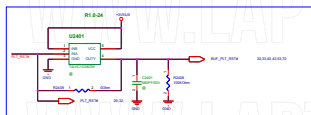
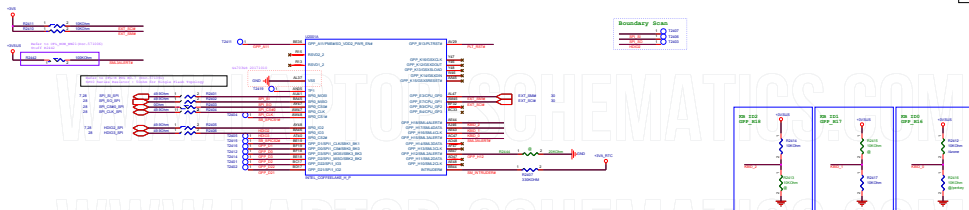
Main Board





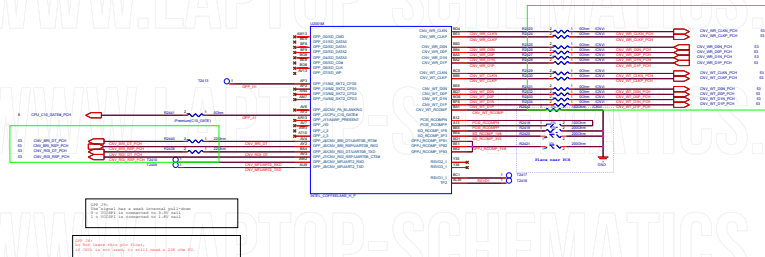


ASUS		Project Name	Rev
Title :		GL703GS	R1.4
Size	Dept.:	ASUSTek COMPUTER	Engineer: EE
Date: Tuesday, January 30, 2018	Sheet	23	of 101



PCB Side (PCB 請在此處查看設計指南)				
Codex	NOG RGR KB Type	KB0 1 (GPP, H12)	KB0 1 (GPP, H12)	KB0 0 (GPP, H12)
000	Non-RGB	M	M	M
001	RGB per Region via (QW6L/6K52) module	M	M	L
002	RGB per Region via 4 zones	M	L	M
009	RGB per key	M	L	L

5. 需請 BIOS RD 在 KB ID 讀取的部分, 額外加入 **Reverse code**, 以符合第 1 點 table



A diagram of a 2D hexagonal lattice. A central blue hexagon is labeled "2D Lattice" and "1". It is surrounded by six red hexagons, each labeled "2". The lattice is part of a larger structure, with a red line extending to the right and a blue line extending to the left.

PCH_GPPB21 : GC6FBEN_PCH

```
PCH_GPPC21 : GPU_RST#
PCH_GPPC20 : DGPU_PWROK
```

PCH_GPPB20 : GPUEVENT#_PCH

	Hynix (2Gb)	XXX (2Gb)	Micron (2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			

PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

PCB_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

	US	UK	JP
KB_LANG_ID0 (KB pin33)	1	0	0
KB_LANG_ID1 (KB pin34)	0	0	1

US.PDN 33 NC , PDN 34 OND
UK.PDN 33,34 OND
JP.PDN 33 OND , PDN 34 NC

		Project Name GL703GS		Rev R1.6
Title : PCH_GPIO				
Size B	Dept.: ASUSTek COMPUTER INC.		Engineer: NB1 R02 EE1	
Date: Tuesday, January 30, 2018			Sheet 25	of 101

Group	Power gain	Power option	Power plane
GRP_A	VCCGRPAPPA	3.3V	+5VDD
GRP_B	VCCGRBPBPA	3.3V	+5VDD
GRP_C	VCCGRPCPCA	3.3V	+5VDD
GRP_D	VCCGRPDPA	1.8V or 3.3V	+5_VDDIO
GRP_E	VCCGRPEPPA	3.3V	+5VDD
GRP_F	VCCGRFPFA	3.3V	+5VDD
GRP_G	IOVDDIO, VDDIO, VDDIO2	IOVDDIO, VDDIO, VDDIO2	+IOVDDIO, +VDDIO, +VDDIO2
GRP_I	VCCGRIPPIPA	3.3V	+5VDD
GRP_J	VCCGRJJPJA	3.3V Only	+5VDD
GRP_K	VCCGRKKPA	1.8V Only	+1_VDDIO
GRP_L	VCCGRLLPA	3.3V	+5VDD
GRP_M	VCCGRMPMA	3.3V Only	+VDDIO, +VDDIO2

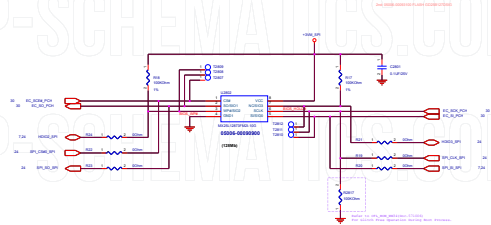
Purple reference C8
Blue reference E8E

ASUS		Product Name	Model
		GL70C3GR	GL70C3
128GB - PCH: POWERD3D2			
Serial	Dept: ASUSAN OPERATIONS INC.		Engineer: NOEL AGUIRRE
Date: 12/04/2013 09:00		Time: 09:00	Page: 1

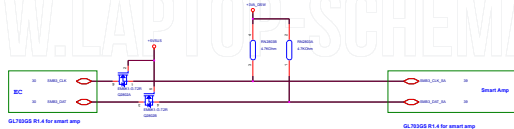
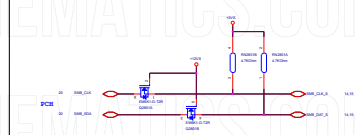
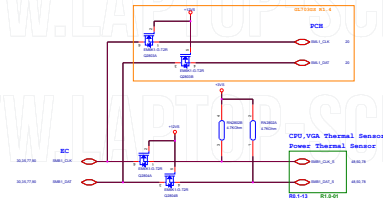




1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M S09-BL

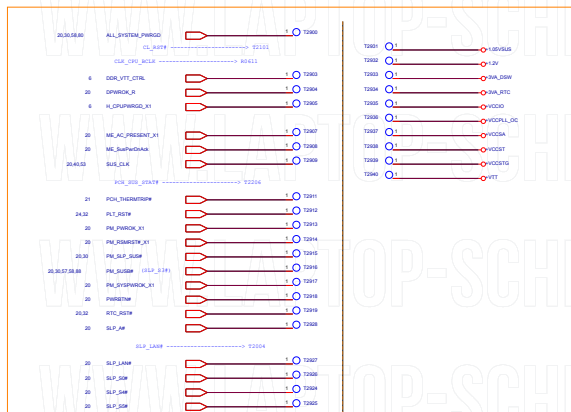


SMBus Interface



Main Board

For power sequence measurement



ASUS		Project Name:	Rev:
GL703GS			01.0
Title : PCH.XDP			
Size:	Dept.:	ASUSTek COMPUTER	Engineer: EE
Date: Tuesday, January 26, 2016	Sheet:	26	of 101

EC 8225

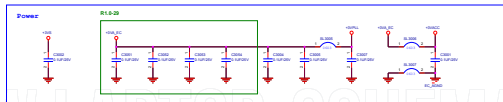
Only 3V Tolerance

GPR[0,1,2,3,4,5,6]
GPR[0,4,6,7]
GPR[4]
GPR[5,7]
GPR[10,17]
GPR[0,17]

Can be adjusted to
Open-drain for port:

GP0-GP3
GP0-GP7
GP0-GP17
GP0-GP7
GP0-GP17
GP0-GP6
GP0-GP17

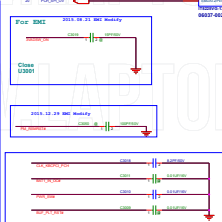
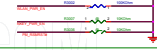
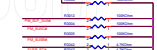
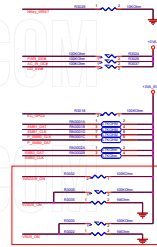
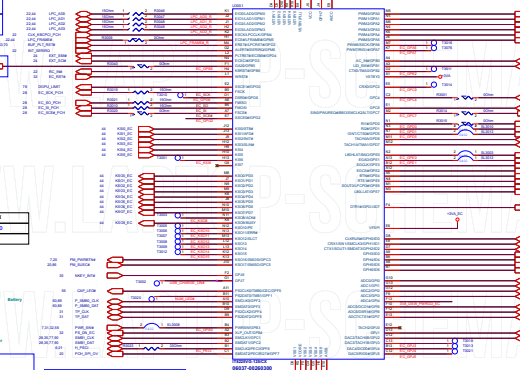
EC Regulator



PG/PG

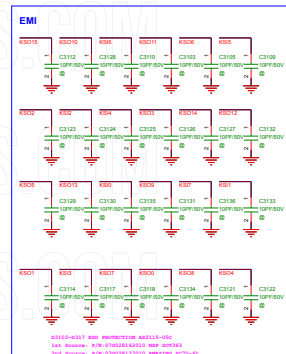
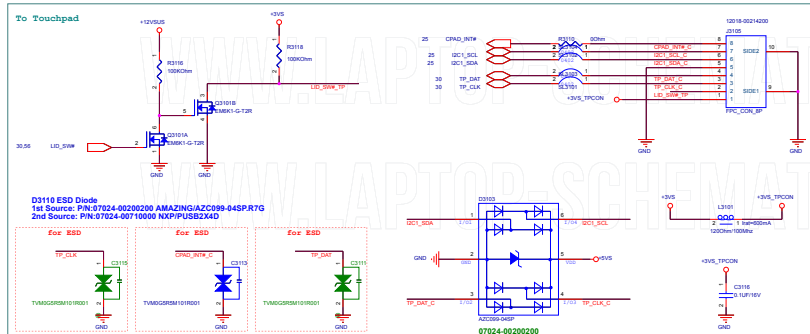
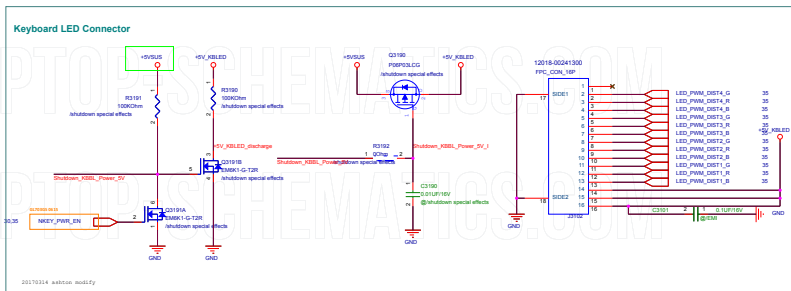
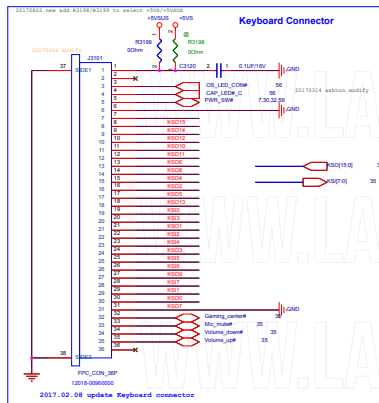


ETE Version	ASUS P/N
2013-09-21/06	06037-0000000

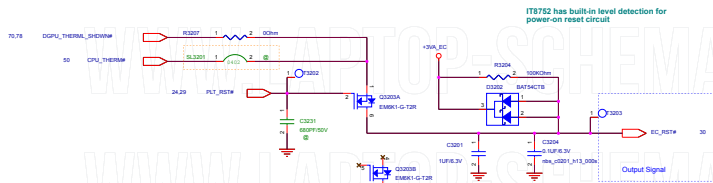


ASUS		Project Name	GL703GR
TR06	EC 8225	Engineer	MBI P00 001
Date:		2013-09-21/06	2013-09-21/06

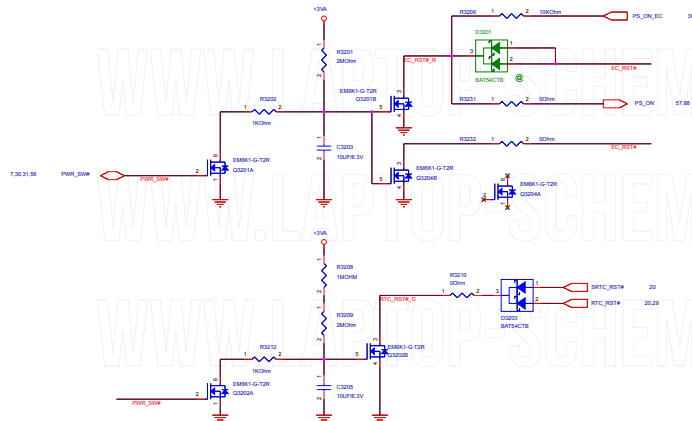
Main Board



Thermal Policy



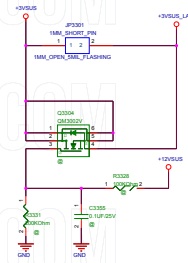
battery embedded (press pwr_sw 10sec, then reset ec)



Project Name		Rev.
GL703GS		R1.4
Title : RST_Reset Circuit		
Size	Dept.:	ASUSTAK COMPUTER INC. Engineer: NB1 RD2 EE1
Date: Tuesday, January 30, 2018	Sheet	32 of 103

2nd: P/N:07G010952500 HOSONIC/E3FB25

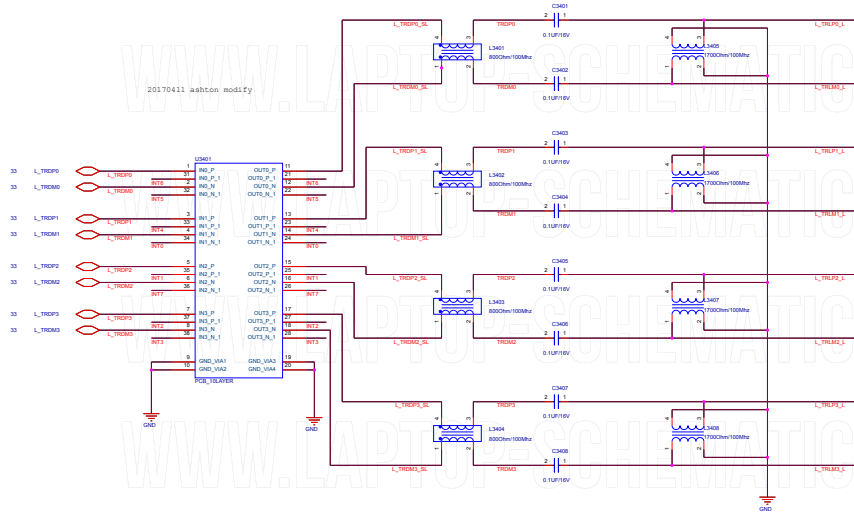
Realtek suggests 3V_LAN raise time >1ms



		Project Name GL703GS		Rev R1
Title : LAN RTL8111GUX-CG				
Size B	Dept.: ASUS&K COMPUTER INC.		Engineer: EE	
Date: Tuesday, January 30, 2018		Drawn	13	of 102

Main Board

LAN Connector



[illegible][illegible]

Diagram illustrating a 10-bit bus system with 10 parallel channels. Each channel consists of a 10-bit shift register and a 10-bit output bus. The channels are labeled Channel 0 through Channel 9. The output buses are connected to a common bus system.

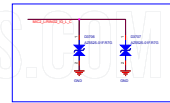
20170710 0000 Pin Pull Low for Keyboard Flash from 00/00



20170428 mod1

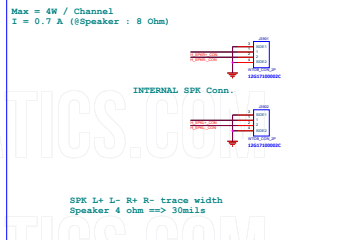
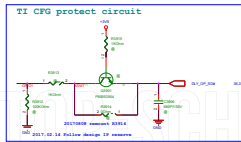


Main Board



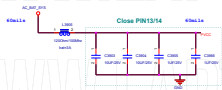
2014.07.22 Reserve DEPOB solution



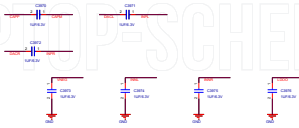
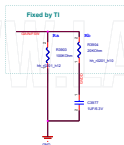


Max = 4W / Channel = 8W
Power Efficiency:85% -> 9.5 W
I=1.05A@9V 0.8 A@12V 0.5A@19V

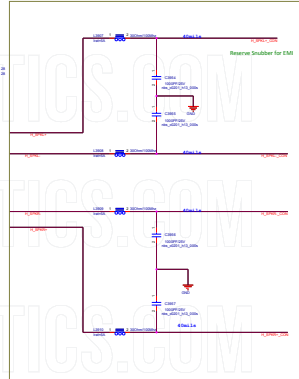
TI_TAS5766M



MLCC 5.22UF025V (60V) 20% 10%

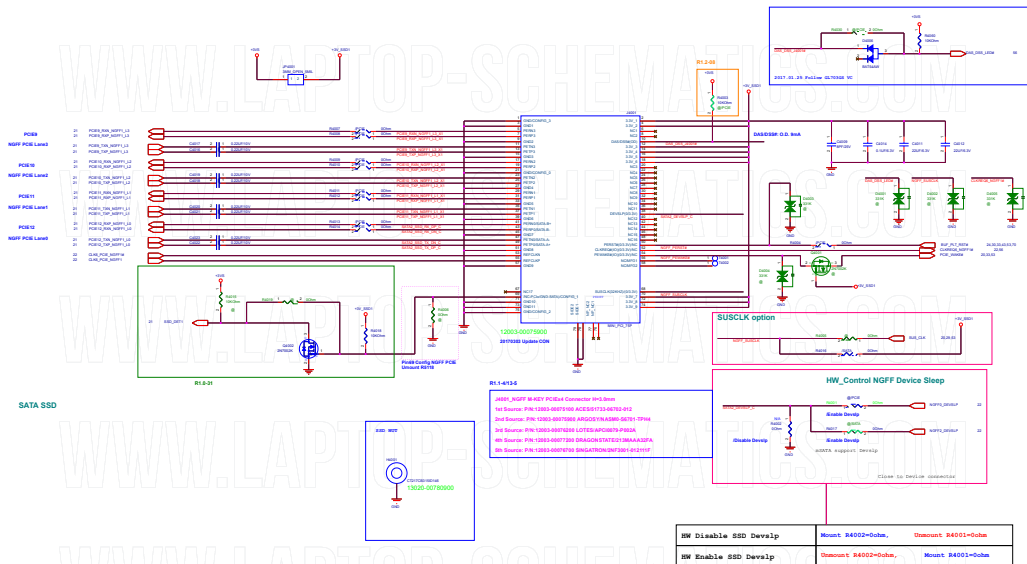


20170808 Modify

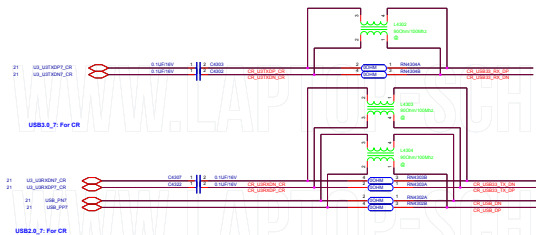


		Title : Aud_Worler
Engineer : EV		
GL703GS		
Date : 2017.08.08		

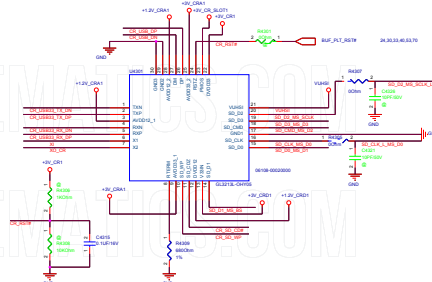
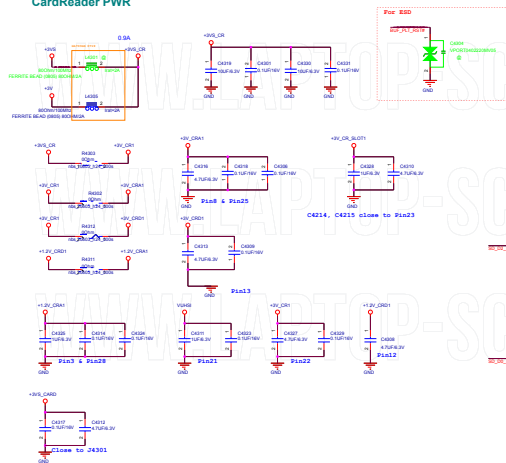
NGFF_SSD



Main Board



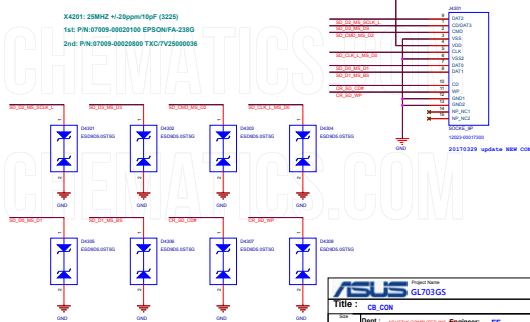
CardReader PWR



CR Socket

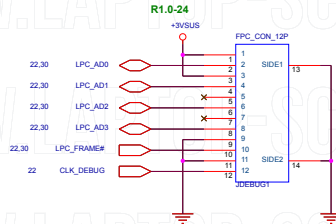


X4201: 25MHZ +/-20ppm/10pF (3225)
1st: P/N:07009-00020100 EPSON/FA-238G
2nd: P/N:07009-00020800 TXC/7V25000036

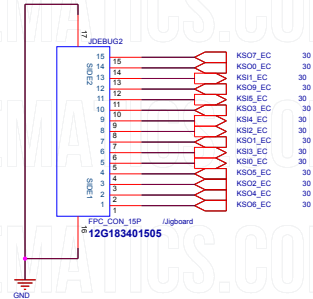


		Project Name GL703GS		Rev R1.0
Title : CB_CON				
Size Custom	Dept.: ASUSTek COMPUTER INC.	Engineer:	EE	
Date: Tuesday, January 30, 2018		Sheet	43	of 101

LPC Debug Port

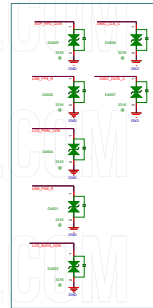
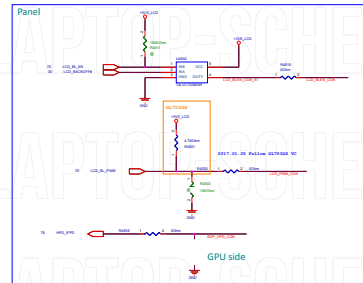


2016/03/21



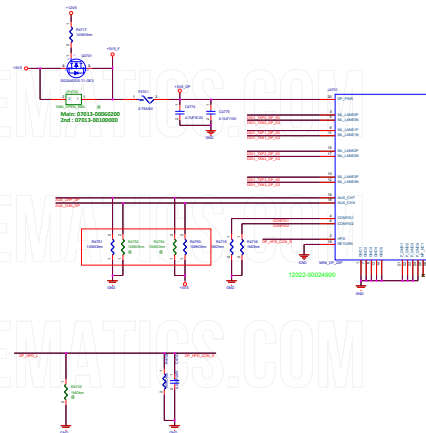
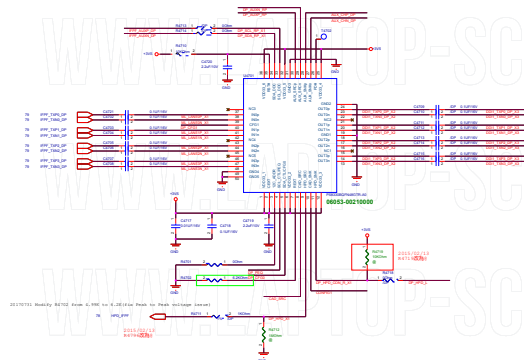
<Variant Name>

ASUS		Title : DEBUG_LPC	
ASUSTek COMPUTER INC. NB1		Engineer: EE	
Size	Project Name		Rev
A	GL703GS		R1.4
Date: Tuesday, January 30, 2018		Sheet	44 of 101

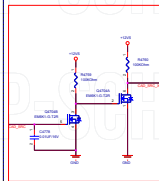
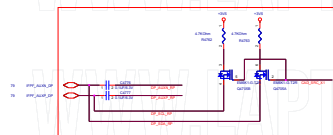


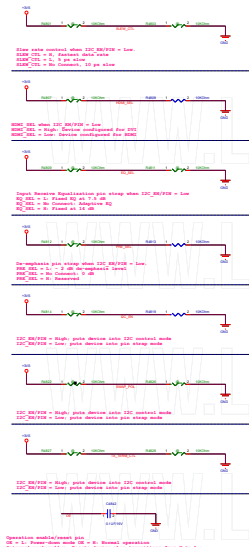
DP Repeater AUX_Sink Input

DP Repeater AUX_SRC Output



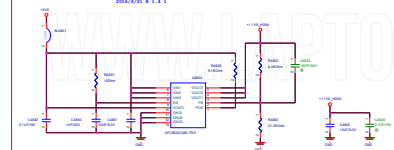
Fix MiniDP to HDMI Dongle No Display Issue



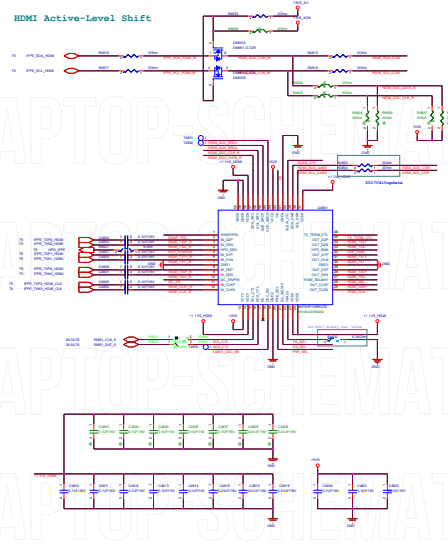


HDMI LDO 1.1VS

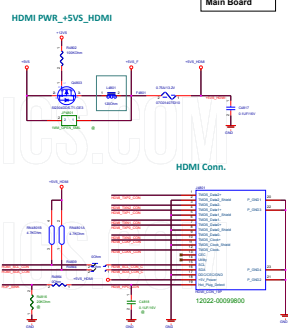
[Download PDF](#)



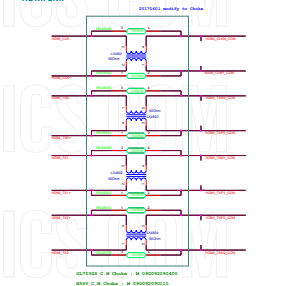
HDMI Active-Level Shift

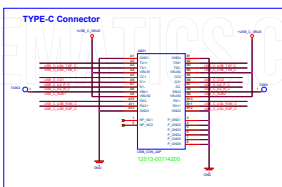
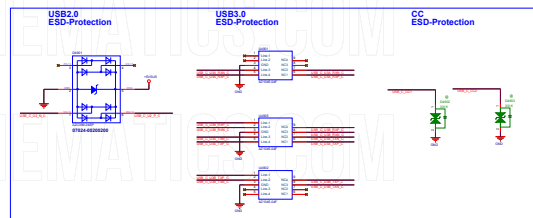
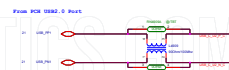
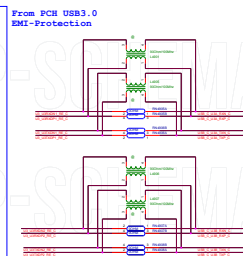


HDMI PWR_+5VS_HDMI



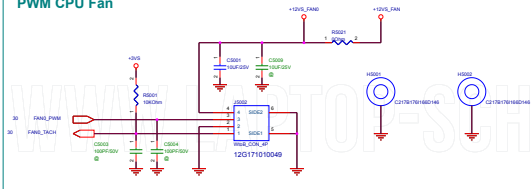
HDMI EMI



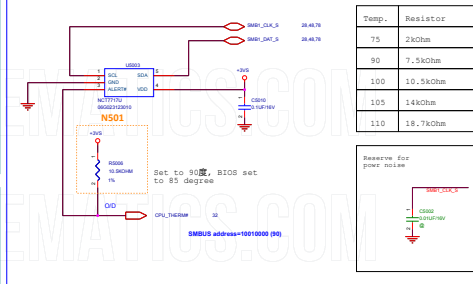


CHG	CHG_H	CC CAPABILITY BROADCAST	CURRENT LIMIT (Typ)	LOAD DETECT THRESHOLD (Typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.05 A

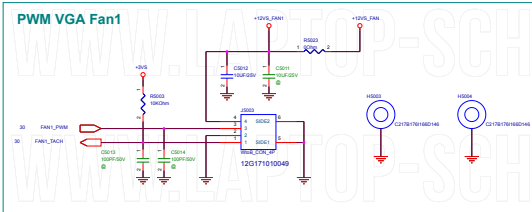
PWM CPU Fan



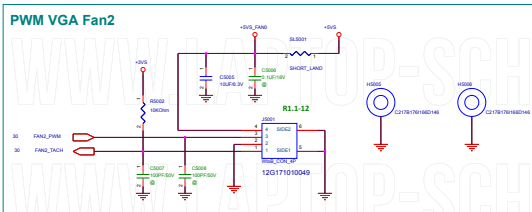
CPU Thermal Sensor

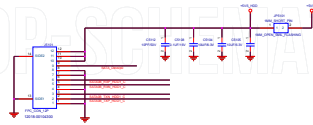


PWM VGA Fan1



PWM VGA Fan2

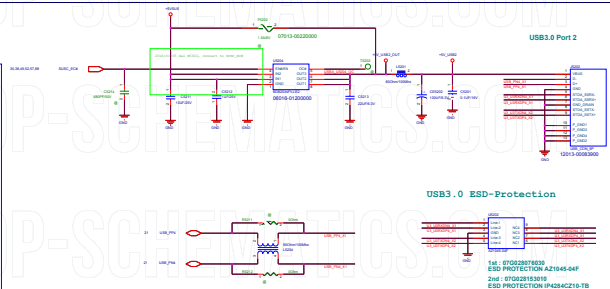
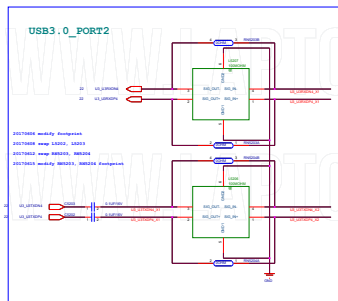
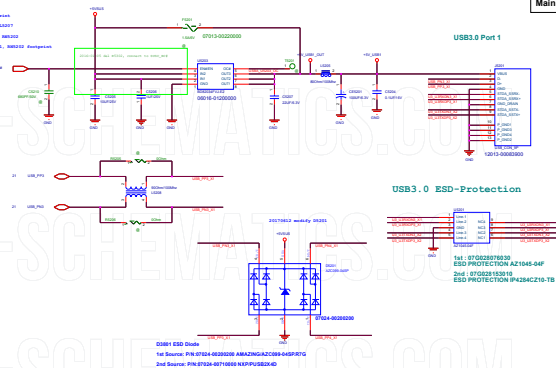
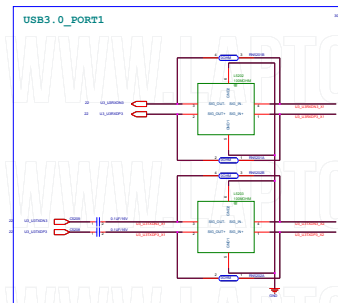





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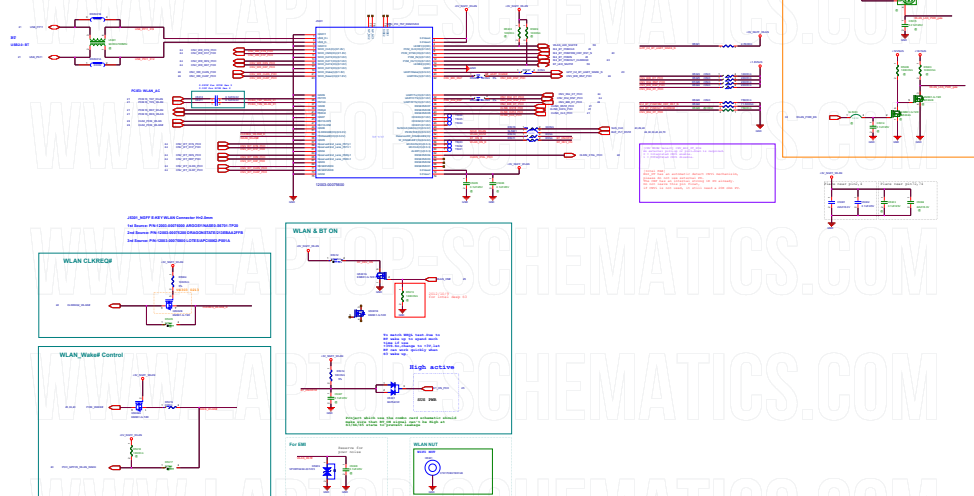
10070406 modify footprint
10070408 swap L3204, L3207
10070412 swap HW3201, HW3202
10070418 modify HW3201, HW3202 footprint

```

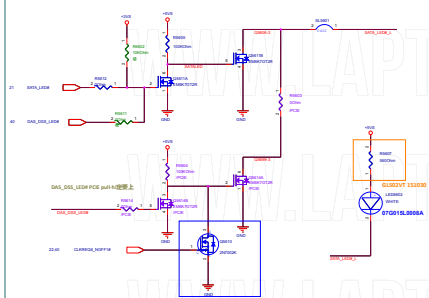


		Title : USB Charger
ASUSTeK COMPUTER, INC. (NI)		Engineer: EE
Site C	Project Name GL703GS	Rev 1.0

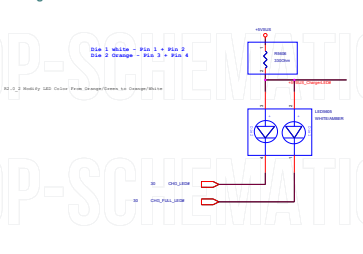
Main Board



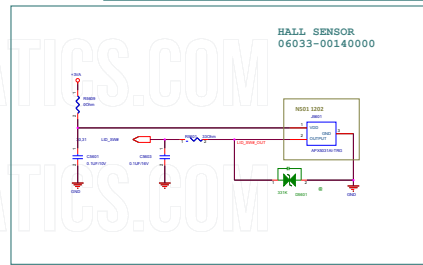
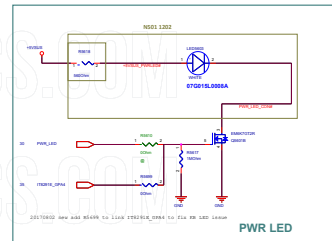
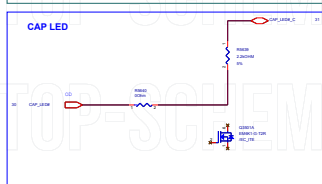
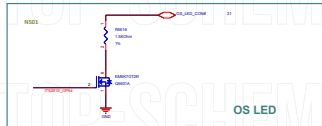
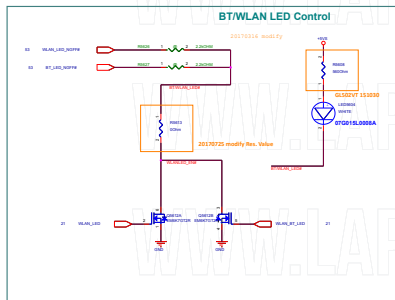
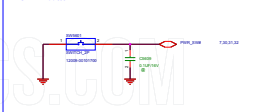
HDD LED & PCIE SSD LED

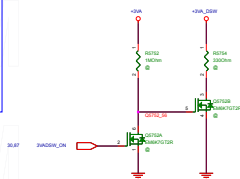
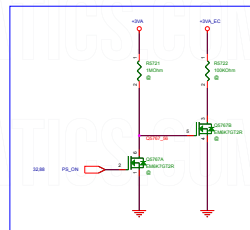
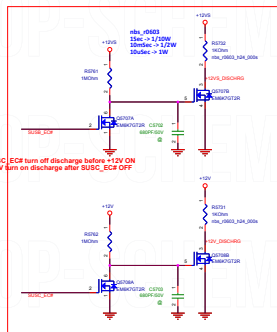
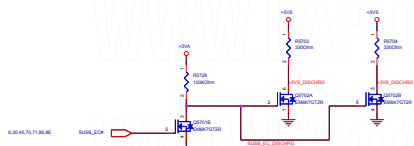
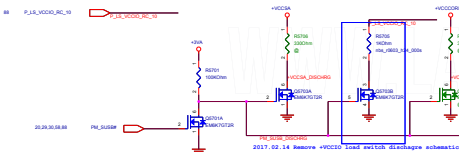


Charger LED



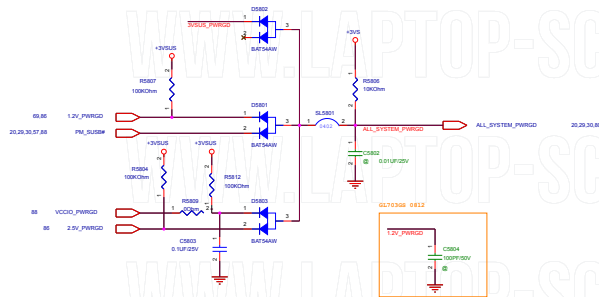
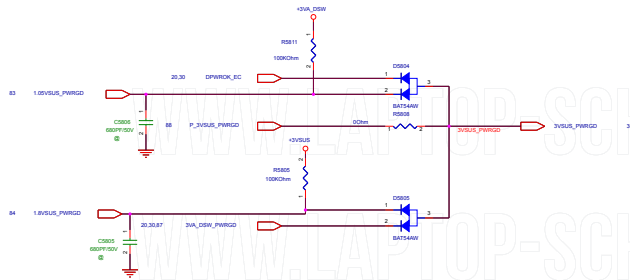
POWER button



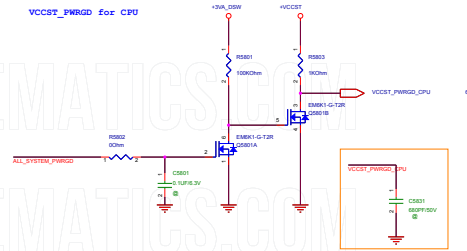


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ASUS		Title : DSG Discharge	
ASUS Inc. COMPUTER		Engineer: EE	
Site	Project Name	GL703GS	Rev
Client	Customer		Rev
Date	Issued	2017.02.14	Rev

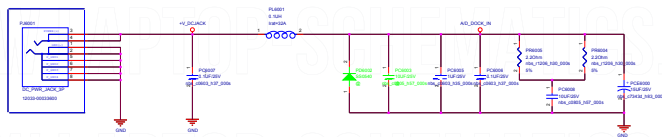


VCCST_PWRGD for CPU



Project Name		Rev
ASUS GL703GS		R1.4
Title : Power Protect		
Size	Dept.: ASUS&TW COMPUTER INC	Engineer: NB1 RD2 EE1
Date: Tuesday, January 30, 2018	Sheet	18 of 101

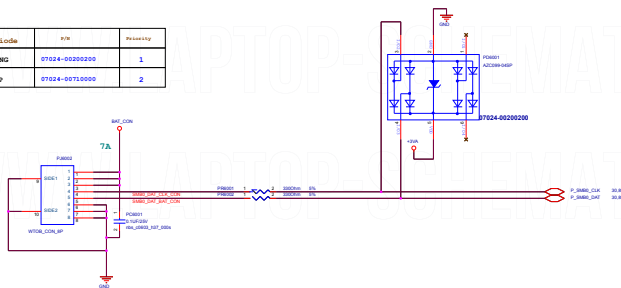
DC-IN Connector



瓦數	P/N (With Cable)	P/N (W/O Cable)	Pin# 數量
120W	14024-00040000	12033-00031000	5
180W	14024-00040000	12033-00031000	7
230W	TBD	12033-00030400	8
330W	TBD	12033-00050100	09602X102300

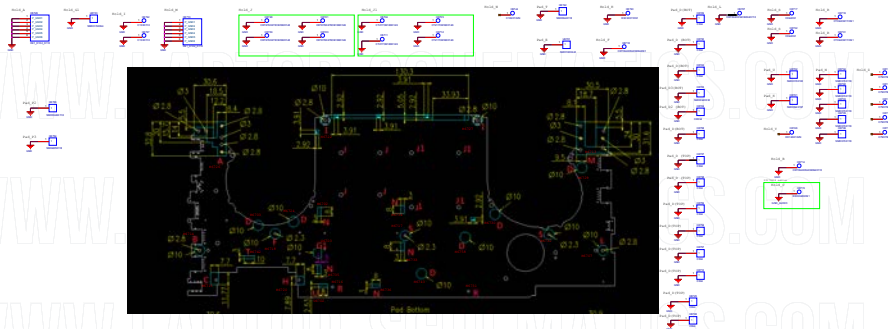
Battery Connector

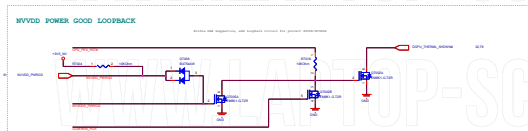
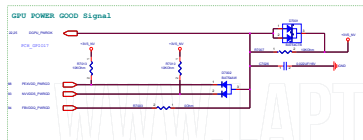
ESD Diode	P/N	Pinout
AMAZING	07024-00200200	1
BCP	07024-00710000	2



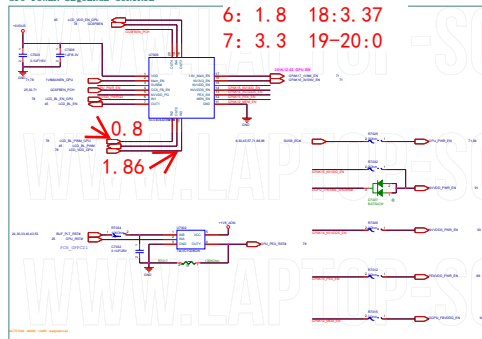
Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

Project Name		Rev.
GL703GS		001
Title : DC & BAT IN		
Size	Dept.: US, Power team	Engineer: Joe
Date: Thursday, June 16, 2017	Draw	60 of 103



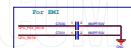
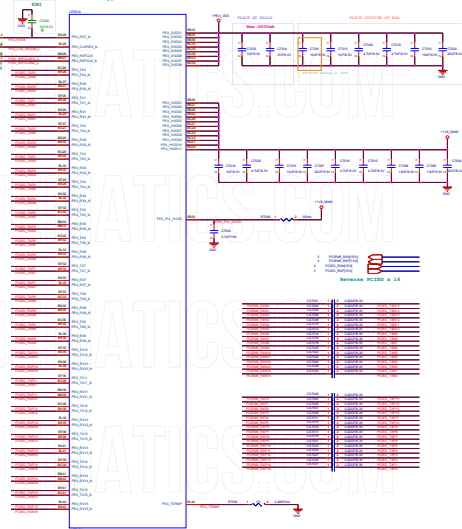


GPU POWER SEQUENCE CONTROL

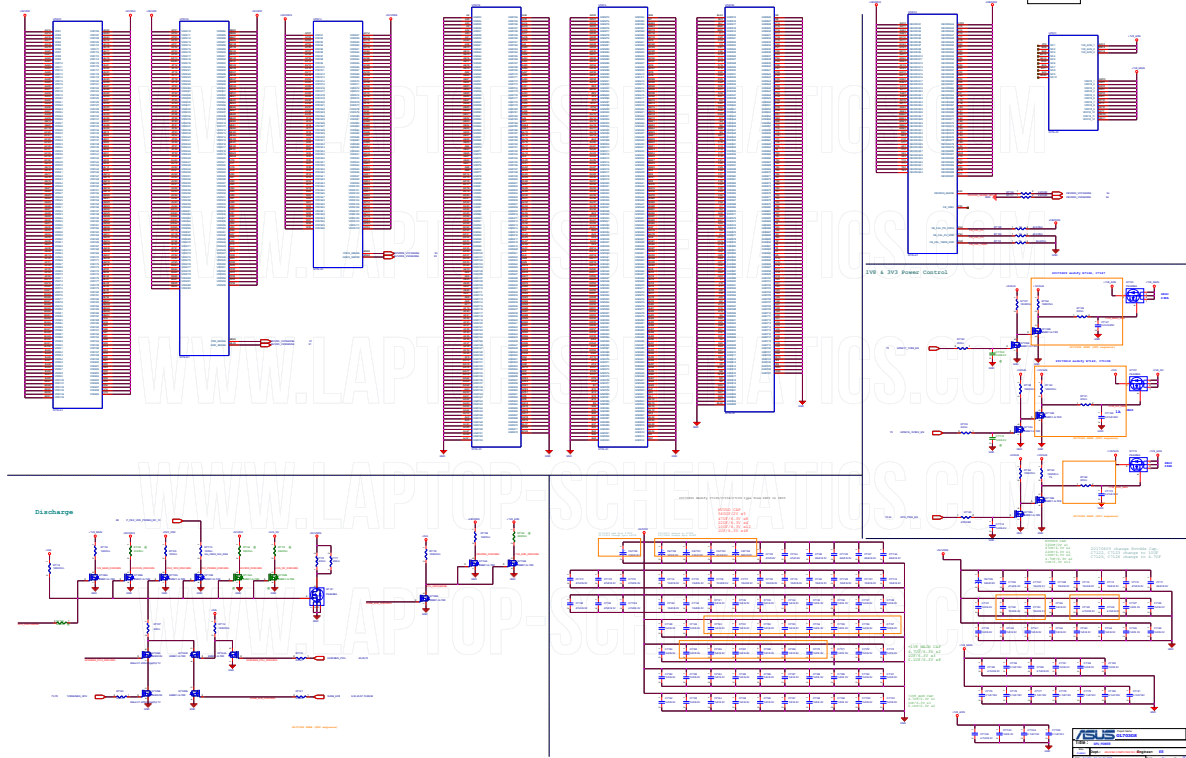


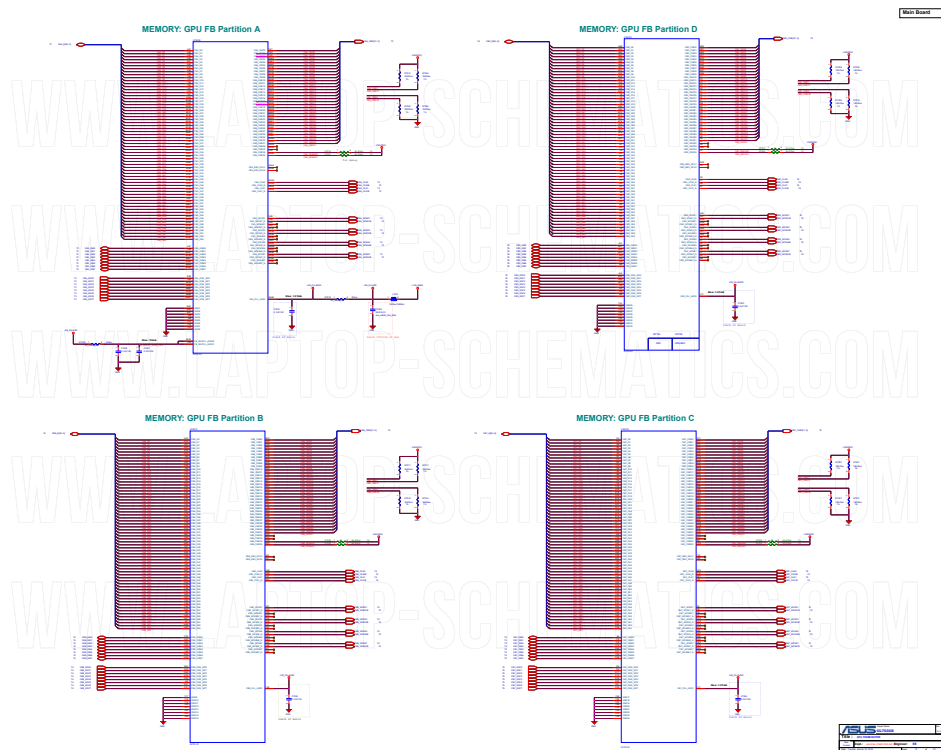
2: 1.8 12:3.37
4: 0 13-17:3.3
6: 1.8 18:3.37
7: 3.3 19-20:0

PCI EXPRESS_Graphics REVERSED Type PCIe X16



Main Board

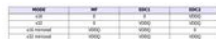




MF=1 Mirror



H5GQ4H24AJRR4C-707A





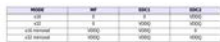
HOUSE	WIF	HOUSE	HOUSE
430	2	2	4000
431	2	4000	4000
432 (revised)	4000	4000	2
433 (revised)	4000	4000	4000



MF=1 Mirror



MF=0 Normal



MF=1 Mirror



MF=0 Normal



3rd: P/N:03008-00030-600 Micron/EDW4032SABG-60-F (B-die) ,Strap: 6x4

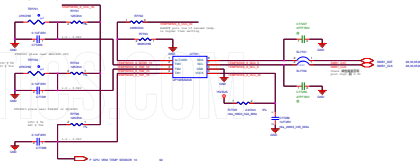
Model	RM	RM-1	RM-2
1.0	0	0	0.000
1.1	0	0.000	0.000
1.2 (normal)	0.000	0.000	0
1.3 (normal)	0.000	0.000	0.000

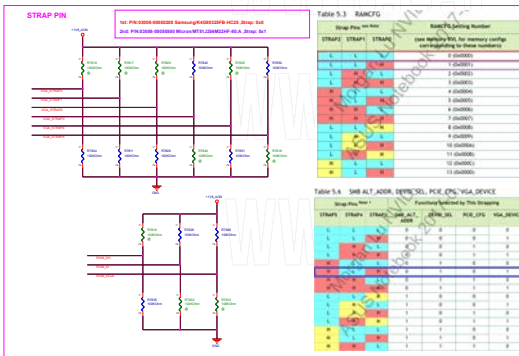
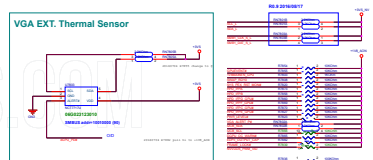
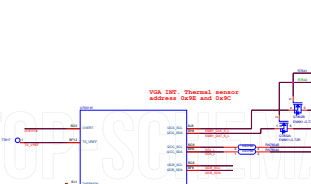
Model	RM	RM-1	RM-2
1.0	0	0	0.000
1.1	0	0.000	0.000
1.2 (normal)	0.000	0.000	0
1.3 (normal)	0.000	0.000	0.000



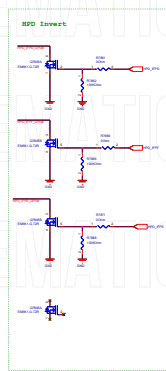
[illegible]

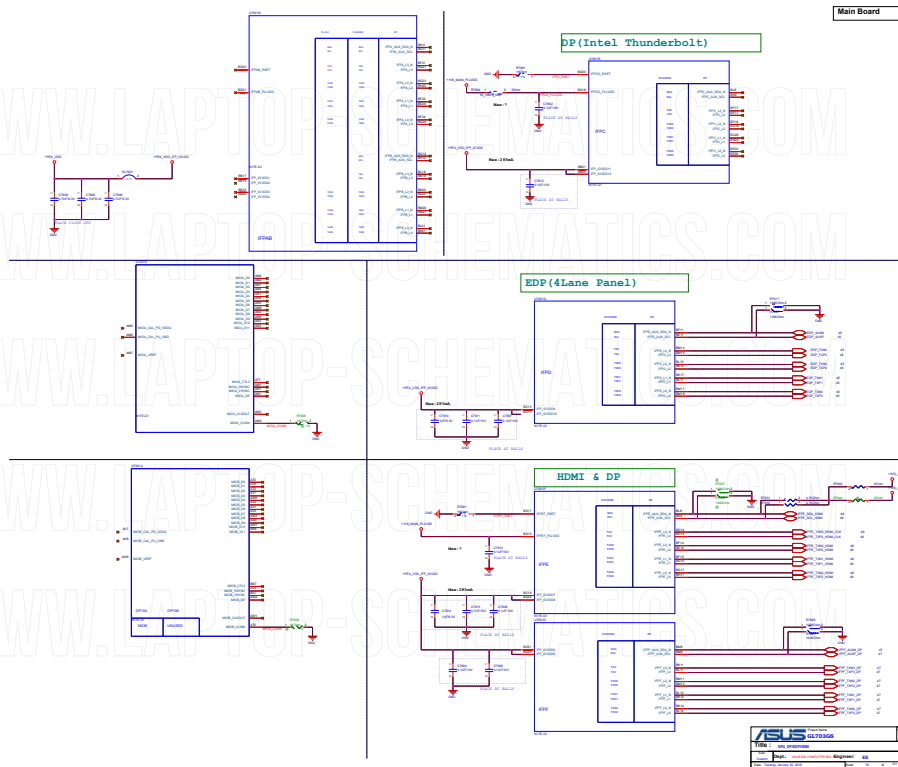
FIGURE 1. (a) α = 0.05, β = 0.05, γ = 0.05, δ = 0.05. (b) α = 0.05, β = 0.05, γ = 0.05, δ = 0.05.

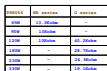


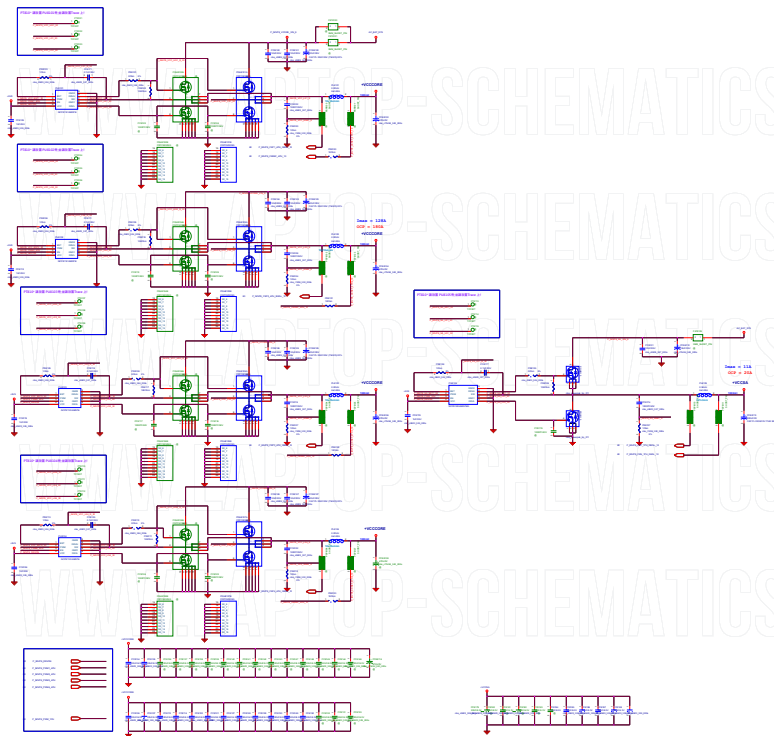
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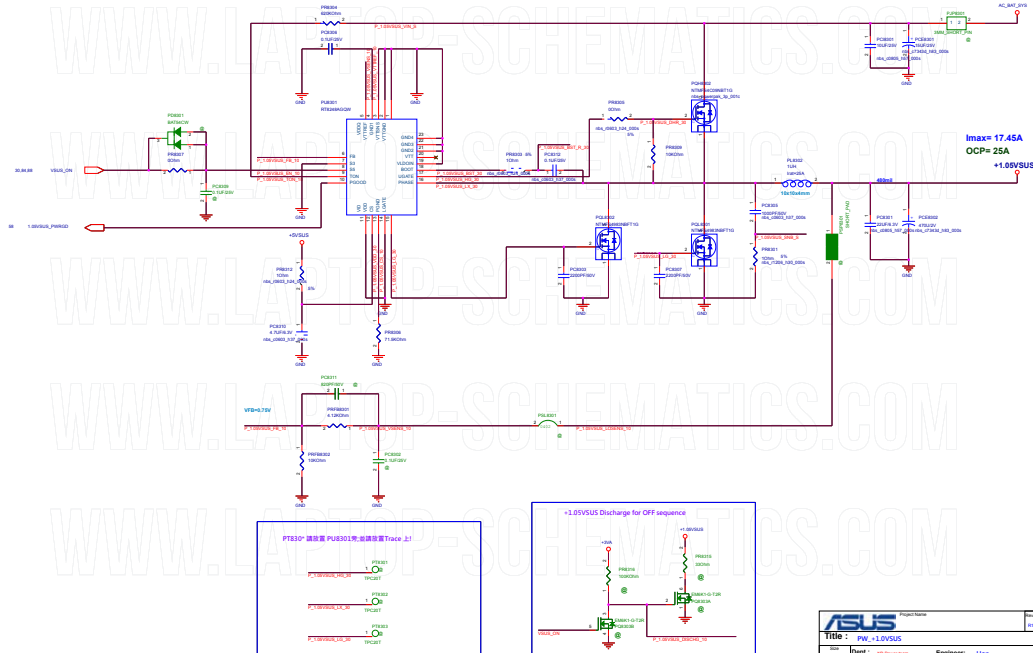
Step 0: Step 1: Step 2:		Functionality Enabled by This Step			
STRAP1	STRAP0	SMI_ALT_ADDR	DEPRN_CTL	PCIe_CFG_VGA_DEVICE	SMI_CFG_VGA_DEVICE
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0



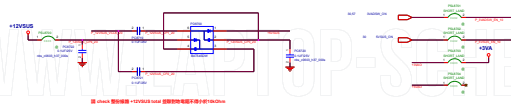
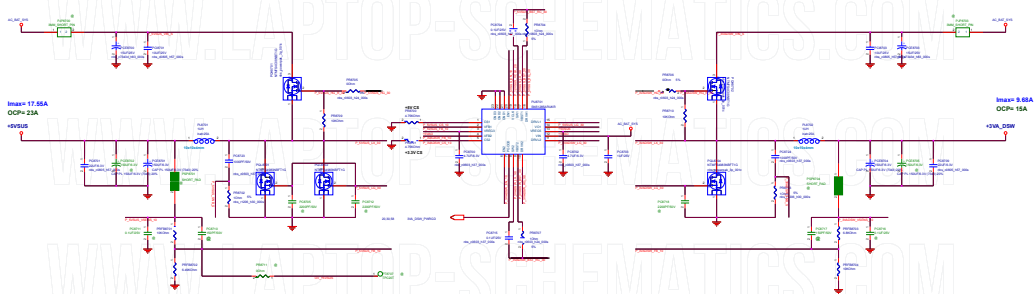








		Project Name		Site	
		GL703GS		In. #	
Title : PW...+L.VSUS					
In. #		Dept.: ntl Power Team		Engineer: Hon	
Date: Sunday, January 26, 2016		Sheet		84 of 103	

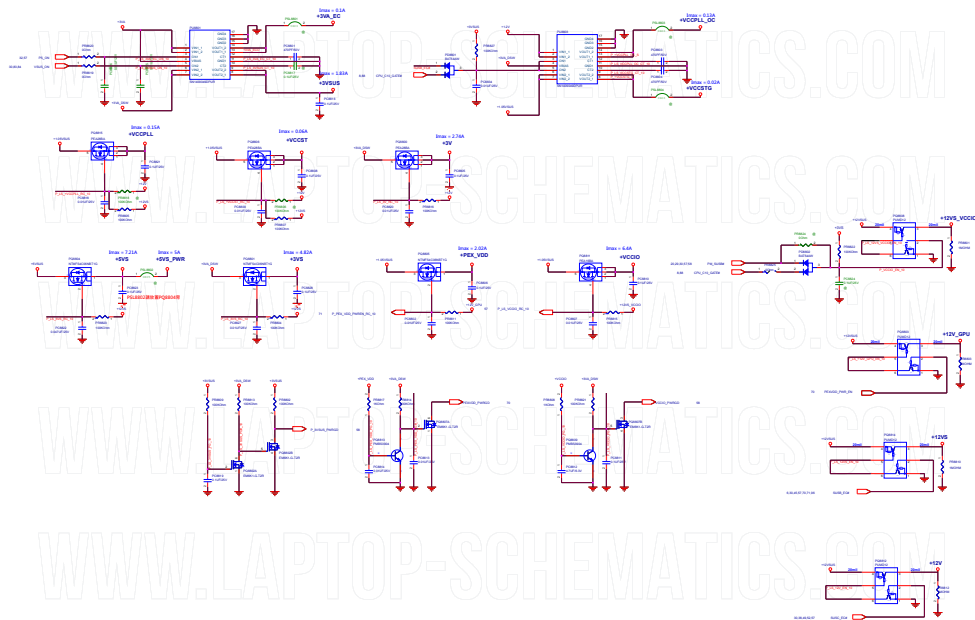


Adaptor Mode (MVP)						
	SB	CB	DB	DB2	SB	SB with USB Charger
PS_ON	0	0	0	0	0	0
PSWAKE_ON	0	0	0	0	0	0
STANBY_ON	0	0	0	0	0	0
SBWAKE_ON	0	0	0	0	0	0
1200V_ON	0	0	0	0	0	0
BUS1_SCA	0	0	0	0	0	0
BUS2_SCA	0	0	0	0	0	0

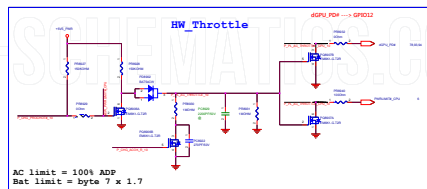
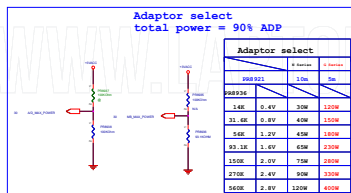
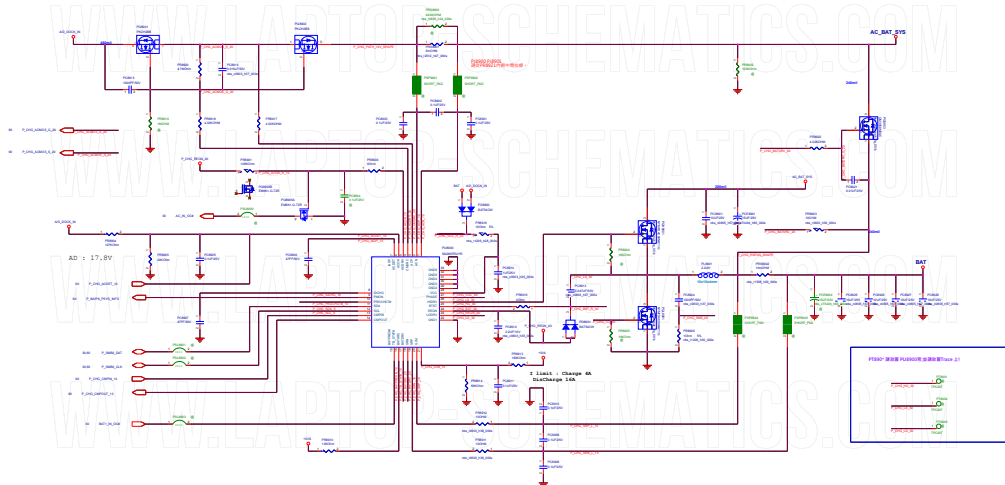
[illegible]

Client Name		Project Name		Rev	
ASUS				01	
Title :		FW_3.0V10.0			
Date		Dept.: RD Power team		Engineer:	
01					
10/1/2010				01 01 00	

Main Board

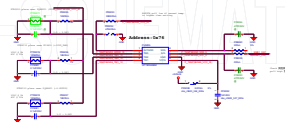
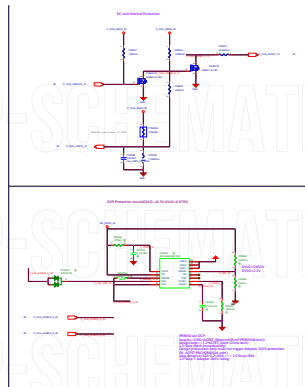
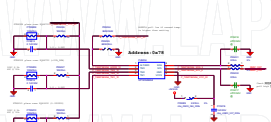
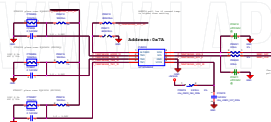
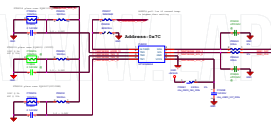
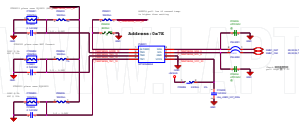


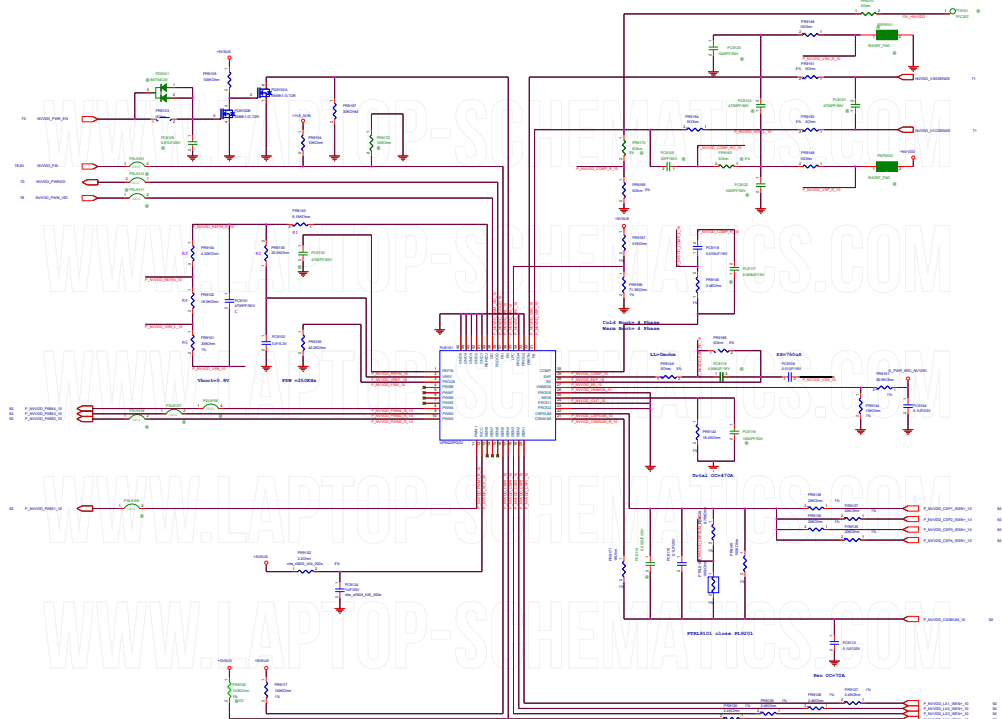
	<=150W	<=230W	>230W	>330W
PRZ8901	10m	5m	5m	2m
	0.06x0.06x0.15-0.25 14	0.06x0.06x0.15-0.25 14	0.1x0.1-0.08x0.08 10	0.1x0.1-0.08x0.08 10

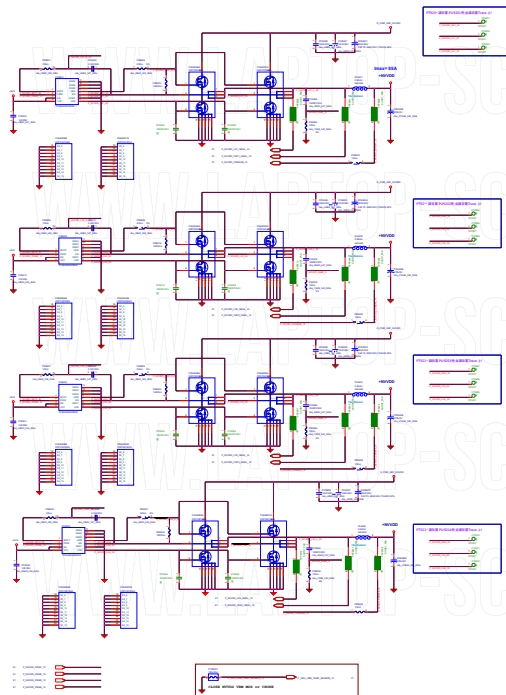


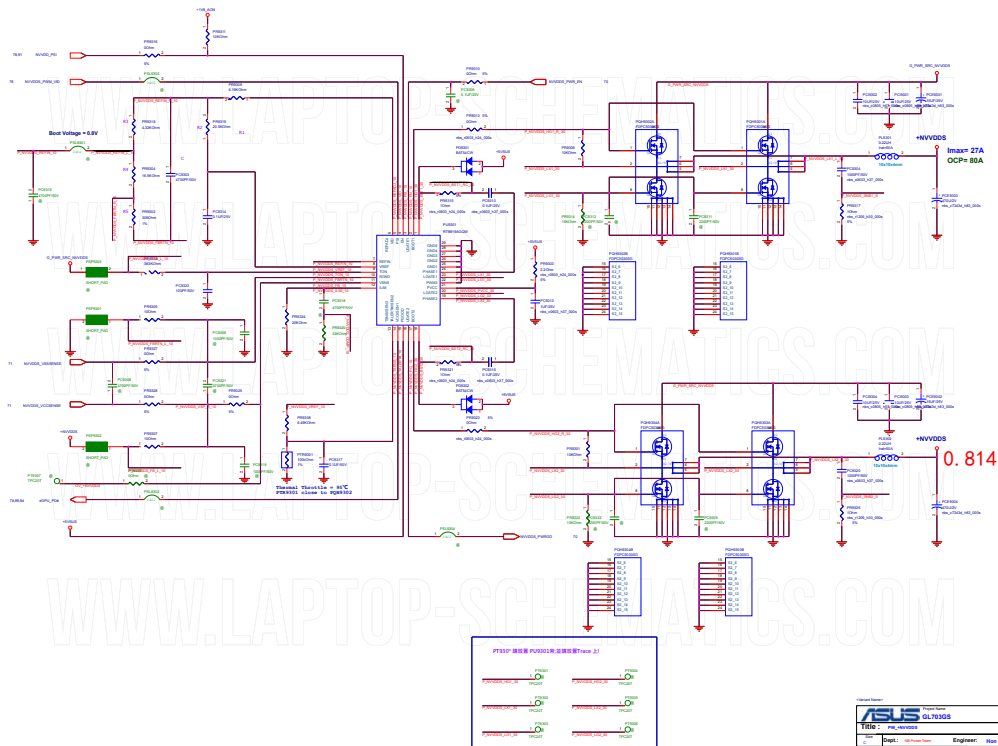
Address	High/Low	Value
0x00000000		
0x00000001		
0x00000002		
0x00000003		
0x00000004		
0x00000005		
0x00000006		
0x00000007		
0x00000008		
0x00000009		
0x0000000A		
0x0000000B		
0x0000000C		
0x0000000D		
0x0000000E		
0x0000000F		

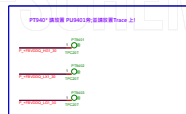
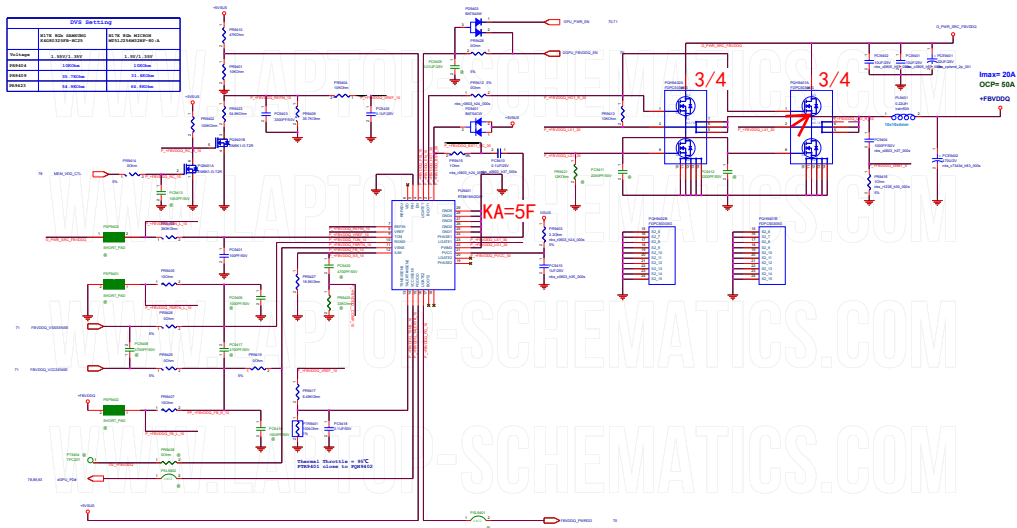
Register	Address	Value
0x00000000		
0x00000001		
0x00000002		
0x00000003		
0x00000004		
0x00000005		
0x00000006		
0x00000007		
0x00000008		
0x00000009		
0x0000000A		
0x0000000B		
0x0000000C		
0x0000000D		
0x0000000E		
0x0000000F		

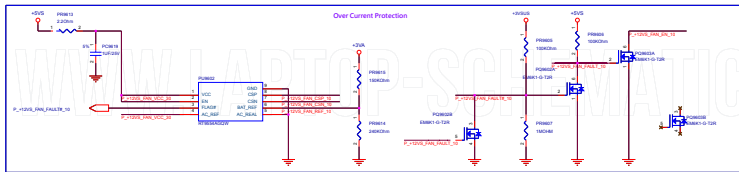
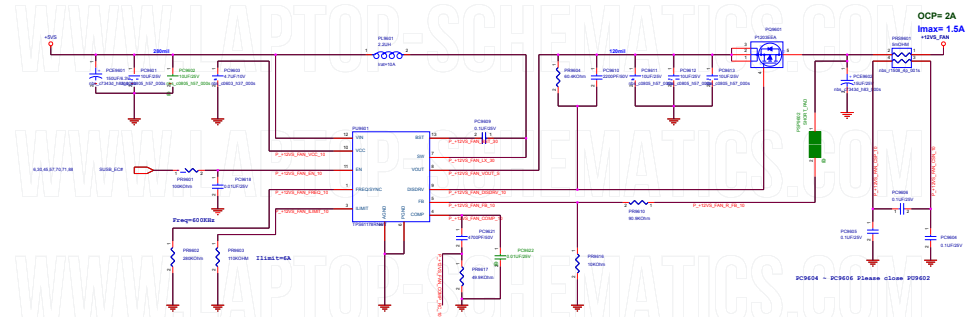




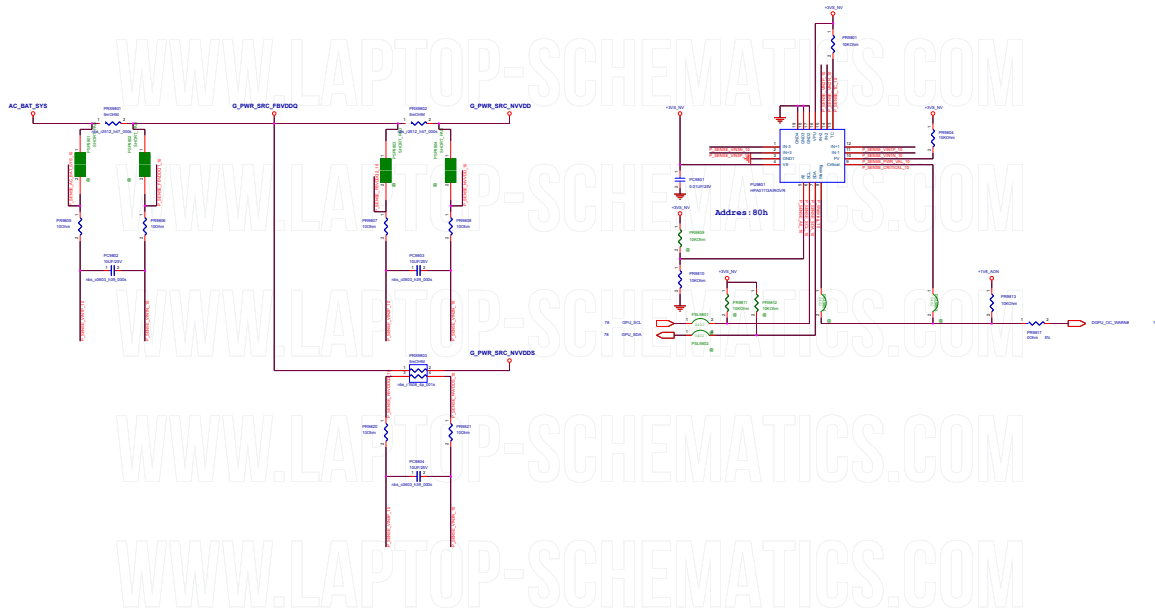


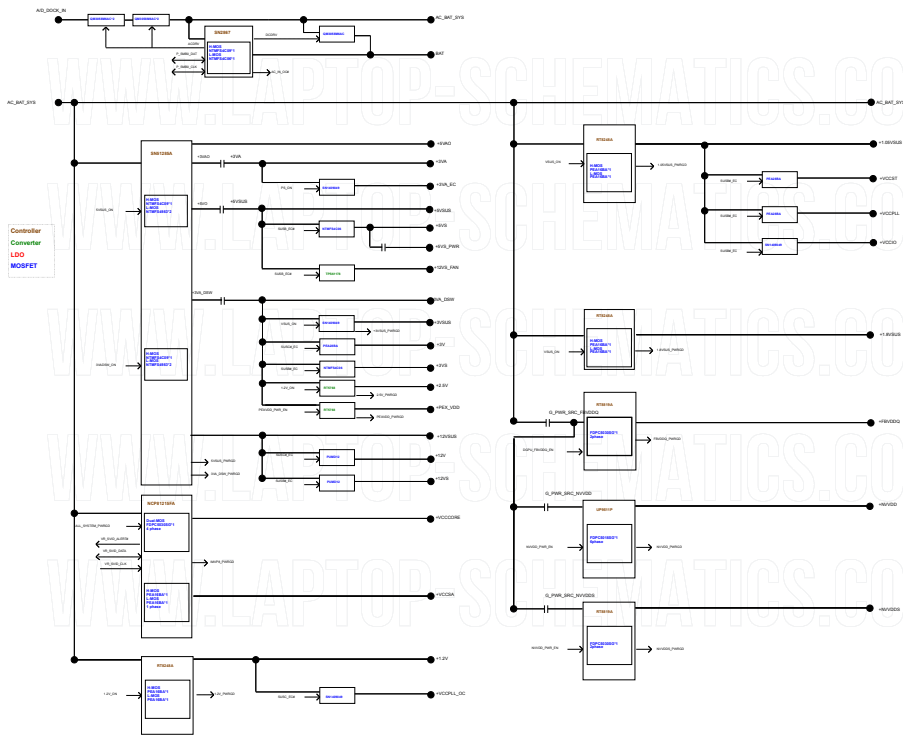






Project Name		Rev	
GL703GS		01.0	
Title : PW_12VDC_FAN			
Des	Dept.	Enginer	Man
Draw	Check	Rev	01



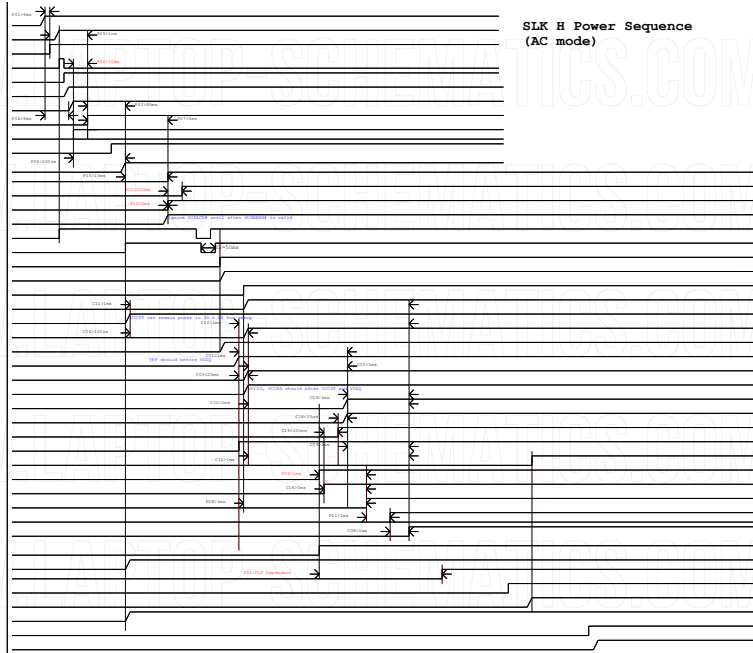


AC-IN Mode

C: CPU
P: PCM
S: PLT
Power
Signal

(+VTCBAT) +3VA_BTC
(AC_BAT_S0) +3VA/+3VA
(+3VA_BTC) R0CST# (PCM)
(Power) AC_IN_D0# (EC)
(EC) R0_O# (+3VA_BTC)
(R0_O#) +3VA_BTC (EC)
(3VAD0H_O#) +3VA_D0H (3VA_D0H_PWR0D)
(EC) D0W0R_EC (PCM)
(+3VA_D0H) R0_BATL0W# (PCM)
(PCM) R0_SL0# (EC)
(V0S0H_O#) +1.0V0S0_V0C0P0C0K (1.0V0S0_PWR0D)
(EC) R0_B0R0S0T#_3CH (PCM)
(PCM) S0S0A0R0H (EC)
(EC) R0_A0_P0R0S0T#_3CH (PCM)
(EC) PCM_S0S0A0C# (PCM)
(PWR_S0L0C#) PWR_O# (EC)
(EC) R0_PWR0S0T# (PCM)
(EC) S0S0C_R0# (Power)
(S0S0C_R0#) +12V/+5V/+3V
(EC) S0S0B_R0# (Power)
(S0S0B_R0#) +1.2V/+5V/+3V
(V0S0H_O#) +1.0V_V0C0P#_V0C0L0 (V0C0P#_PWR0D)
(+V0C0C0) +V0C0C0
(1.2V_O#) +1.2V (1.2V_PWR0D)
(1.2V_O#) +V0S0C_C0 (1.2V_PWR0D)
(+12V0) +V0C0L0_O0
(S0S0B_R0#) +V0C0C0 (V0C0C0_PWR0D)
(ALL_SYSTEM_PWR0D) +V0C0C0 (1M0P#_PWR0D)
(S0H_VTT_C0L0) +0.6V
(C0P0) S0H_VTT_C0L0 (Power)
(Power) 1.2V_PWR0D (AMD)
(Power) 1M0P#_PWR0D
(AMD) ALL_SYSTEM_PWR0D (C0P0/PCM/EC/Power)
(ALL_SYSTEM_PWR0D) V0C0P#_PWR0D_C0P0
(EC) PWR_PWR0D_P0# (PCM)
(PCM) C0L0_P0#_R0C0L0 (C0P0)
(PCM) H_C0P0_PWR0D (C0P0)
(ALL_SYSTEM_PWR0D) P_1M0P#_R0_10 (Power)
(C0P0) P_1M0P#_R0_10 (Power)
(EC) PWR_PWR0D_P0# (PCM)
(PCM) P0L0_R0T# (C0P0/EC/Device)
(P_1M0P#_R0T#) +V0C0C0R0 (1M0P#_PWR0D)
(C0P0) H_0R0R0R0R0P# (PCM)
(PCM) S0R0_0R0R0R0T# (Memory)
+V0C0C0

SLK H Power Sequence (AC mode)



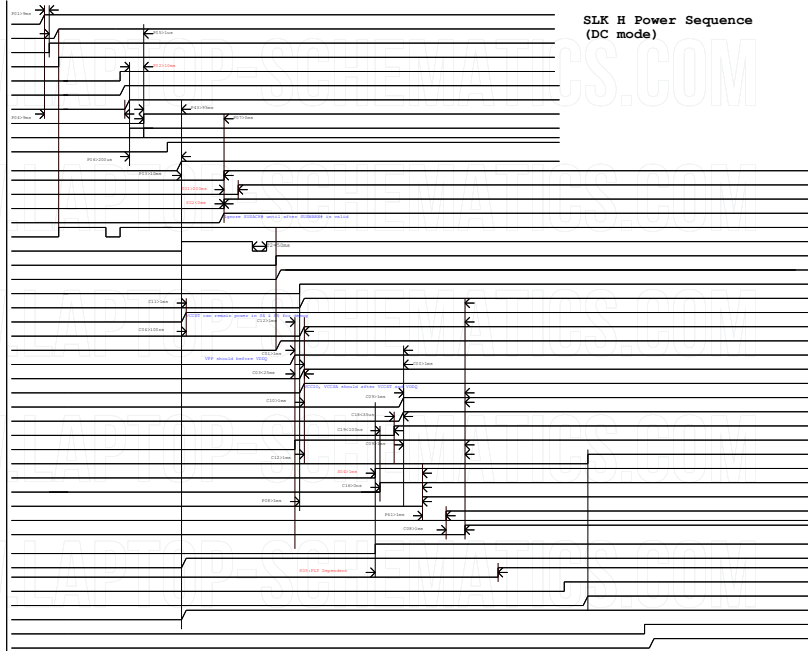
ASUS		Product Name	GL704GS
TBM :		Power On Timing AC mode	
Unit	Signal	Manufacturer	Engineer
MB1 R02 E01			

DC-IN Mode

```

P1CPU                                     +((C0CAT) + (3VA_BDC
P1CPU                                     (AC_BAG_VSD) + (3VA + (3VA
S1PLT                                     + (3VA_BDC) + (C0CAT) (PCR)
Power                                     (Power) AC_2M_DCN (PCR)
Signal                                     (EC) PS_ON + (3VA_BDC)
                                     (PS_ON) + (3VA_BDC) (AC)
                                     (3VADGN_ON) + (3VA_DGN) + (3VA_DGN_FWRGDS)
                                     (EC) DPWDRD_EC (PCR)
                                     (3VA_DSN) PM_BATLON (PCR)
                                     (PCR) PM_SLP_S2SD (EC)
(VSDG_ON) + 1.0VSDG_VCCPWR (1.0VSDG_VSDG)
                                     (EC) PM_RDRSTR_S2SD (PCR)
                                     (PCR) PM_RDRSTR_S2SD (PCR)
(EC) ME_AC_PRRSTR_PCH (PCR)
                                     (EC) PCH_PDR_SACK (PCR)
                                     (PWR Switch) PWR_SW (EC)
                                     (EC) PM_FWRGDRN (PCR)
                                     (EC) S0SC_EC (Power)
(S0SC_EC) + 12V + 5V + 3V
                                     (EC) S0SC_EC (Power)
(S0SC_EC) + 12V + 5V + 3V
(VSDG_ON) + 1.0V_VCCST, VCCPL (VCCST_FWRGDS)
                                     + (VCCST) + (VCCST)
(1.2V_ON) + 2.5V (1.2V_PWRGDS)
(1.2V_ON) + VDDG_CPU (1.2V_PWRGDS)
                                     + (12V) + (VCCPL_OC
(S0SC_EC) + (VCCST) (VCCST_FWRGDS)
(ALL_SYSTEM_FWRGDS) + (VCCSA (DPWR_FWRGDS)
                                     (D0R_VTT_CTRL) + 6.0V
(CPU) D0R_VTT_CTRL (Power)
(Power) 1.2V_FWRGDS (AND)
(Power) DPWR_FWRGDS
(AND) ALL_SYSTEM_FWRGDS (CPU) (PCR) (EC) PCH (PCR)
(ALL_SYSTEM_FWRGDS) VCCST_FWRGDS, CPU (CPU)
(EC) PM_FWRGDRN (PCR)
(CPU) CLR_PCH_CLR_CLR (CPU)
(PCR) PM_FWRGDRN (CPU)
(ALL_SYSTEM_FWRGDS) + (DPWR_EC_10 (Power)
(CPU) P_VSDG_DATA_X2 (Power)
(PCR) PM_FWRGDRN_PCH (PCR)
(CPU) FLT_RST (CPU) (Device)
(P_DPWR_FWRGDS) + (VCCSCOR (DPWR_FWRGDS)
(CPU) H_THERMTRIP (PCR)
(CPU) D0R4_G0R0RSTP (Memory)

```



SLK H Power Sequence (DC mode)

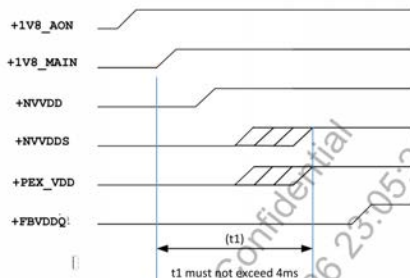


Figure 7.5 Example of Power-Up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2ms.
- t1 (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_PGOOD) must NOT exceed 4ms.
- The ramp-up overshoot should not exceed the silicon reliability limit voltage.
- Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp-up.
- Power up 1V8_AON must be 90% before 3V3 ramp up
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU CANNOT have any 3.3V leakage paths before 1V8_AON is present.
- No signal should be applied to the GPU before power rails are fully ramped.
- Refer to the JEDEC Memory Specification for memory-related power sequencing.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 μ s during both power up and power down.
- FBVDD/Q and 1V8_AON don't need power cycle for GC6 2.1

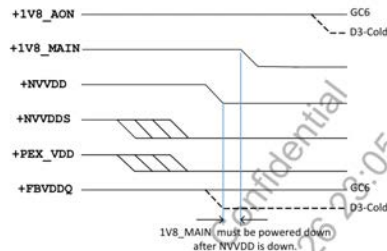
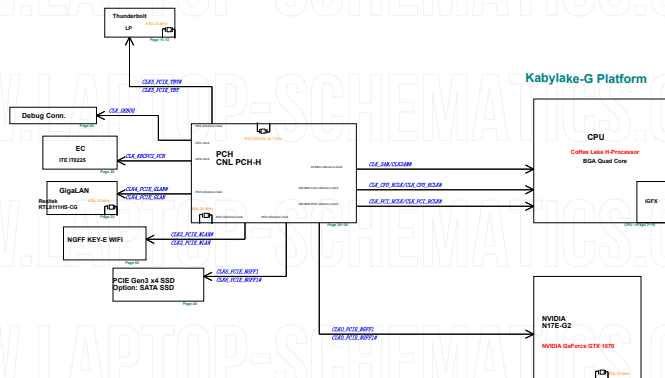


Figure 7.6 Example of Power-Down Sequencing Order

The following power-down sequence is required:

- ▶ NVVDDS/PEX_DVDD must power down before NVVDD; all other power rails can power down together with NVVDD.
- ▶ 1V8_MAIN must power down after NVVDD powers down.
- ▶ The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 μ s during both power-up and power-down.
- ▶ For GDDR5X VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
- ▶ All 3.3V devices that connect to the GPU must be ramped down before 1V8_AON; GPU CANNOT have any 3.3V leakage paths after 1.8V_AON and 1.8V_MAIN power-down.
- ▶ Power down of NVVDDS and PEX_DVDD must be less than 10% before NVVDD can start ramp-down.
- ▶ Power down of 3V3 must be less than 10% before 1V8_AON can start ramp-down.

Clock Distribution Diagram



SMBUS Block Diagram

